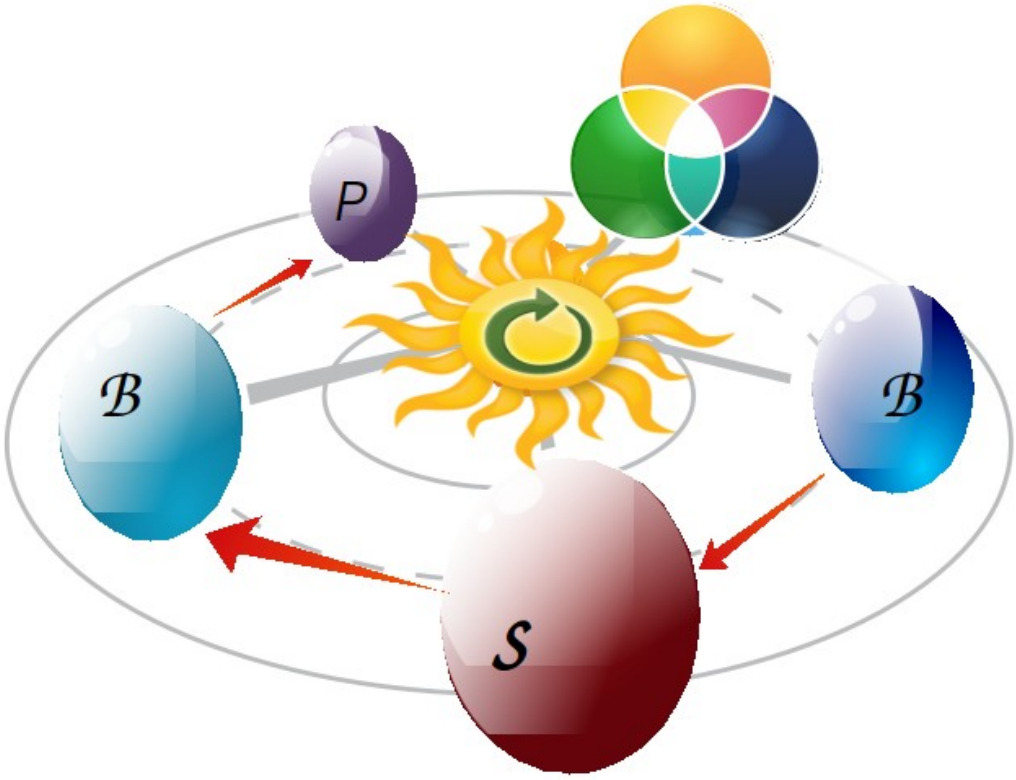


Barrys Scientific Based Products

Barrys Scientific Based Products BIOS Chip ver 1.4

By

Barry L. Crouse

Introduction

I would like to thank you for taking the time in viewing this work. I have designed a new BIOS chip that interfaces with the CPU I have previously designed specifically 576. The CPU 576 is designed for middle range servers small to medium level businesses. The new chip Design offers integration with better security approaches taken. The BIOS chip is a 576 pin wire chip titanium plated with the inside using copper wires and built in Ring topology that offers encryption to protect system level based software. Please be aware I had to scale the side pins to make this design look more aesthetic. The scale is 16 pins represent 32 pins 1 to 2 ratio. The new Bios chip comes with four buffers to process 73728 bits at 128 cycles.. This system is geared more to Linux and Unix based systems.

On a side note, I have registered my package design Patent used on the 1st page in Canada. In regards to the new BIOS chip design, I believe that I have developed a new method or process for BIOS based encryption the equations have been tested three times and should be valid. Chapter 5 presents a short presentation of the Hard Disk and Memory chips configuration coupled with Menu Screen encryption process developed in chapter 4 using 73728 bits using 576 * 128 cycles.

This Rom chip design has been completed for middle grade servers. This Rom Chip version includes using the new BIOS Encryption process that has been designed. I have added the following mouse, key,communications, and micro time fields to this chip design see chapter chapter 5. The menu screen contains is designed for the 576 pin bios chip design with more external devices available for encryption including the keyboard.

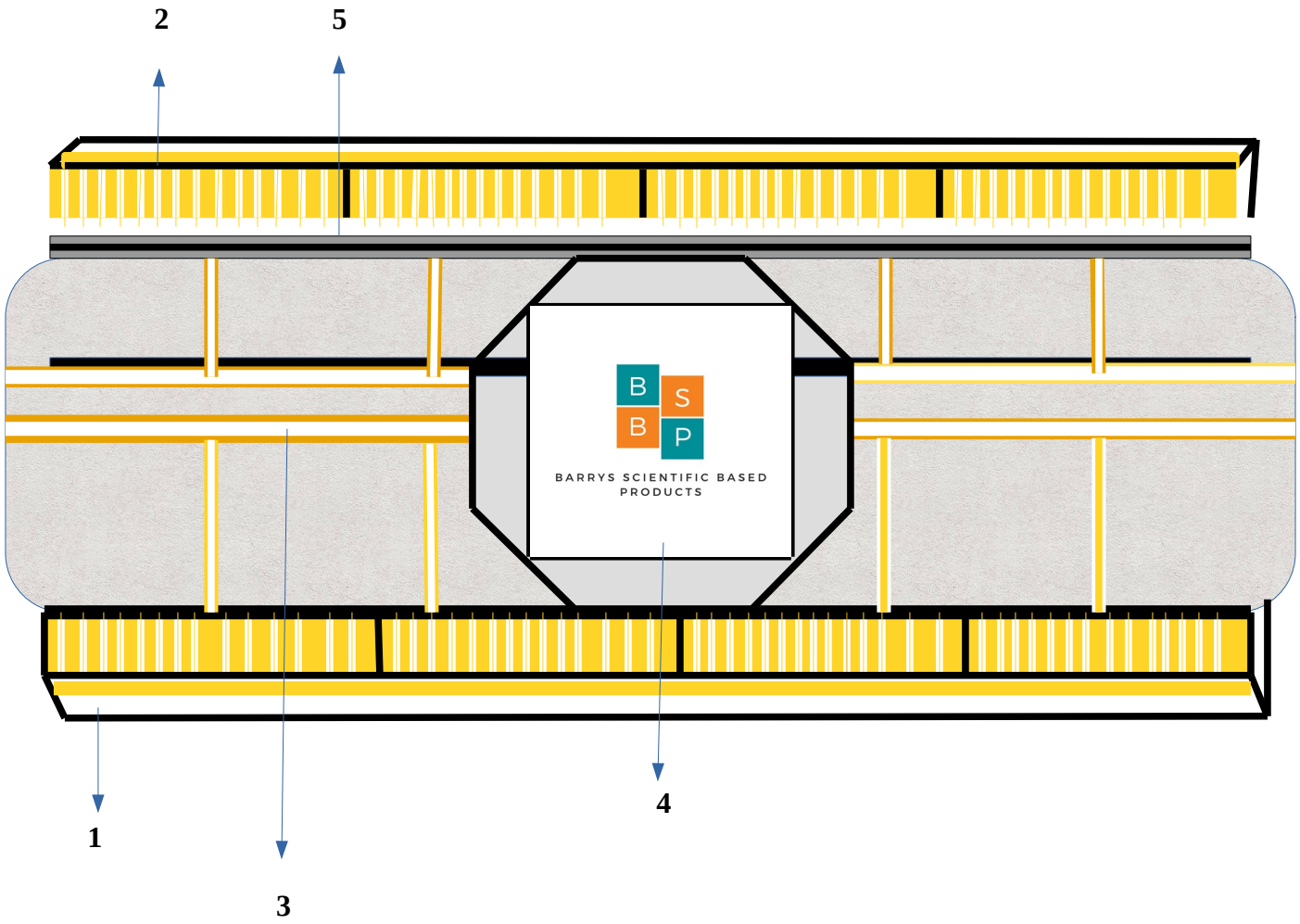
The next progression would have been 512 but that would have followed a predictable pattern and by using 576 this design has some elements of randomness with the encryption process using a prime number 17 making it more difficult in terms of mathematics and Cyber hacking. In Martial arts this is called a feint.

Table of Contents

Visual Design

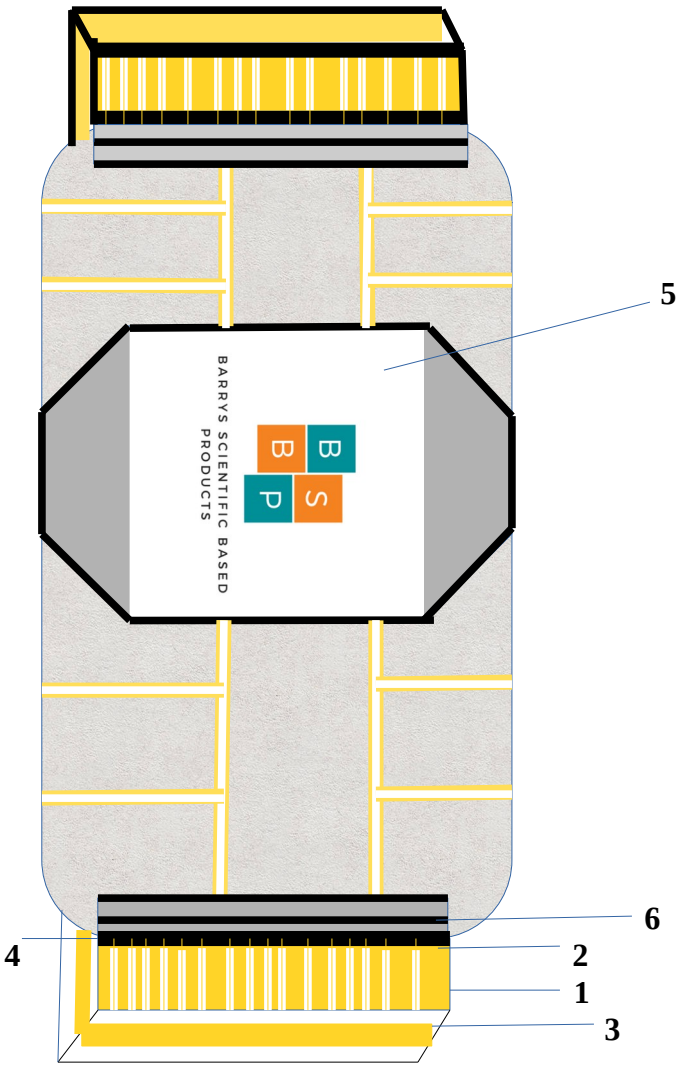
Chapter 1

Bios Chip Design ver 1.4/576 Chart 1-A



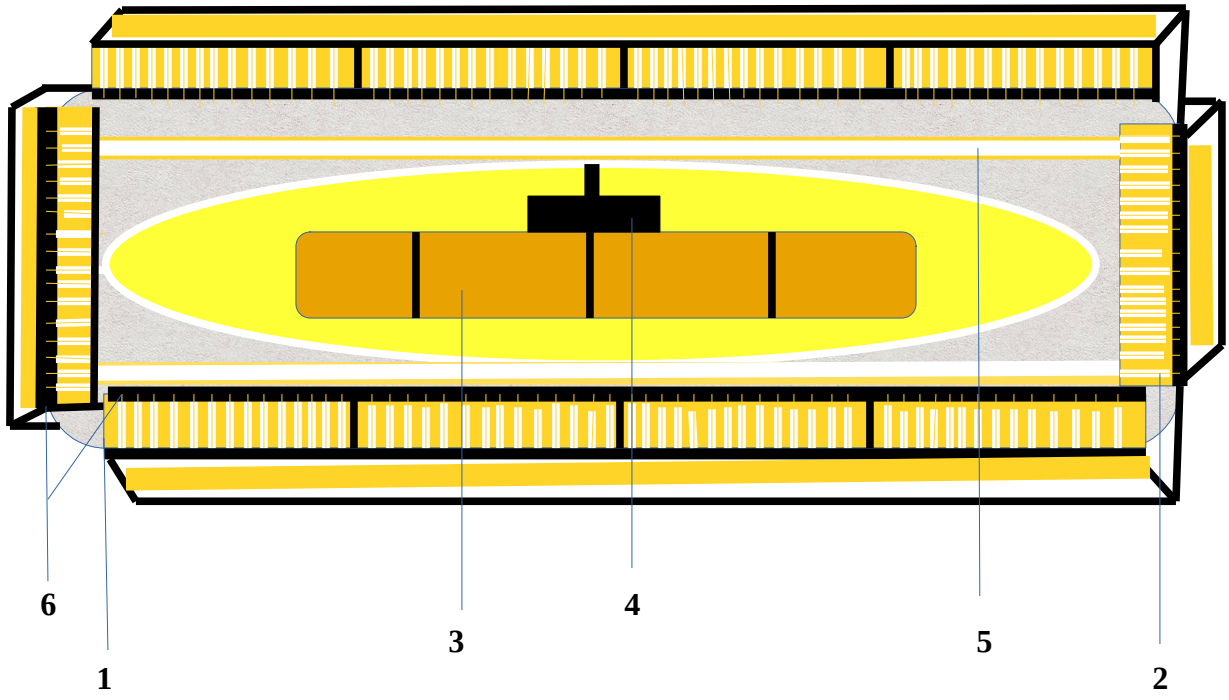
1). Dual sided Pins 56 * 2 = 112 Slot 1 and 2 total 224 .10 cm titanium plated Copper inside
2). Dual sided Pins 56 * 2 =112 slot 3 and 4 total 224 .10 cm titanium plated Copper inside
3). Titanium Plated with thin fiber optic wiring inside.
4). Logo placed on Bios chip
5). Internal Bridge Pins to Fiber Optic wiring

Bios Chip Design ver 1.4/576 Horizontal Pins Chart 2-A



1). 32 pins per side total 128 pins (scaled on chart 2-a 16 pins on Design)
2). Pins .10 Titanium plated copper inside
3). Dual sided bank
4). Heat shield
5). Logo placed on chip
6) Bridge to network paths

Bios Chip Design ver 1.4/576 Chart 3-A Back view



1). Dual sided Pins 56 * 2 = 112 Slot 1 and 2 total 224 .10 cm titanium plated Copper inside
2). Dual sided Pins 16* 2 =32 slot 1 and 2 = 128 .10 Titanium copper plated inside
3). Buffer 4 spaces 32 per cycle total 128 cycles
4). Bridge
5). Data path from and to Pins
6). Heat shields

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 576 pins 112*4 and 32*4 that is dual sided. In chart 1-a I configured the pins are represented by showing the front side of the pins that are dual sided. The side of the chip has a dual side as well. The pin composite is .10 cm Titanium plated outside and copper inside. The design deploys heat shields as well The front side has 4 wires for a total of 8. Wires on the side are not split. The Bios chip is capable of running the CPU I previously designed 576 bits. This allows encryption to take place masking the BIOS and CPU's and now hard disk raided with memory. The encryption ring uses .20 cm making thicker wires to push more bits through.

The BIOS chip also has Thick wires that are copper plated .20 cm titanium inside copper .10 cm along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches.

On the back side of the BIOS chip see chart 3-A has a thick fiber optic ring network topology and four buffers with a way to pipe more bits to the mother board and uses I/O Scheduling allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption process and or method

Encryption method for Password

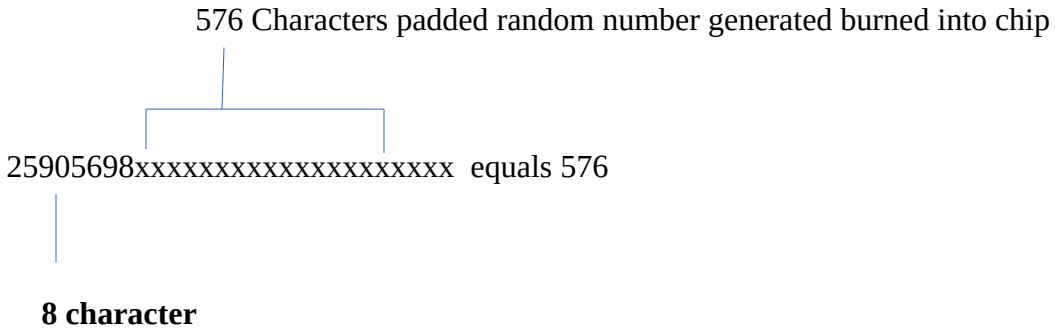
BIOS Pins	# Cycles	CPU used	padded bits
576	8	576	4032
576	16	576	8640
576	24	576	13248

Equation Equals BIOS Pins * Number of cycles minus CPU

BIOS Pins	#CPU	Password field length	Bit Strength
576	576	14	8064
576	576	16	9216
576	576	24	13824

Equation is CPU add padded bits/128 equals password length = Bit Strength

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 4032 Padded Bits plus 576 / 576 equal 8 characters for my security key because I am allowed 576 characters I can than pad the other 568 characters for my security key thus my security key would look like this below:



If I took 9216 plus 576 / 576 I could use 17 characters and 576 minus 17 I can use 559 characters padding also 13824 padded plus 576 /576 equals 25 Characters with 551 character padding. **This is a example of only 1 cycle if you turn to the next page I use 8 cycles for my process.**

Real Characters	**Padded Characters**	**Constant 128**
8	568	576
17	559	576
25	551	576

Security Key Encryption

CPU	Constant = 576 bits	#Characters	Character pad
576	**576**	**8**	**568**
576	**576**	**17**	**559**
576	**576**	**25**	**551**

Equation = 1). CPU*8 /576 = #Characters

A = 576

2). A – Character Representation = Character Padding

This idea would create 3 security keys used for the CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key 576 equals Password Length 576

Each security key is different and unique depending on the encoding scheme used. The Equation takes a CPU multiply by eights divide by 576. The 2nd step is declare A =576. The 3rd step is A – Character representation gives you the amount of padding you can use which represents character representation. because I am allowed a total of 576 characters using the method and adding the padding I can now extend my security keys to 576 characters.

Chapter 4

Menu Screen

Date mm/dd/yyyy/ade **73728 Bits Menu Screen**

Time 000:000:000

Barrys Scientific Based Products BIOS Software

Bios Chip ver 1.4

1). CPU 576 Bits

2). Password Security

3). Raided Disk

4). Hard Disk Encryption

5). BIOS Menu Encryption

6). Memory Encryption

7). USB Device Encryption

8). Mouse Encryption

9). Communications

10). Keyboard Encryption

Bios Menu Screen Updates ver 1.4

The following updates have been applied for this Bios Menu Screen

1). Screen is encrypted using 73728 Bits @ 576 * 128

2). Devices Mouse, Keyboard, Communications have now been added in this version.

3). The time Field has been added with microseconds included This also will protect against server certificates and misconfigurations do to misuse of time fields.

Chapter 5

Hard Disk and Memory Encryption

After reviewing Chart 3-a, I can now create Hard Disk and Menu Screen Encryption because I have a BIOS chip that has a builtin Network Topology Hardware and System level software based on the following parameters:

1). Bios Pins 128 cycles
2). assigned variable 73728 Bits

The Equation is 73728 bits / 128 = 128 cycles based on the hardware using thick wires it would take 128 cycles to encrypt the hard disk whether raided or not and now Memory Chips. This would create bottle necks. The solution is to create four area buffers to load the cycles into the Data Pipe meaning each buffer could load 32 cycles since there are four and would equal 128 cycles. This would alleviate bottle necks by using the I/O scheduling mechanisms for each buffer space.

Chapter 6

Final Thoughts

This Bios chip and was designed for Middle range servers using a 576 bit CPU.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it's number of bits maximum 73728 bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is now using a newly designed mathematical process and or method working with 128 cycles. In previous works, I used the newly designed process and it is now valid because it has been shown to work on three different occasions with this design not using a sequential pattern. I have updated the Menu Screen using this BIOS chip at 73728 bits encrypted.

The BIOS chip uses 576 pins with the backside of the chip using a thicker internal fiber optic ring topology that utilizes encryption to protect the BIOS software. I have created four buffer areas that would allow for hard disk, memory, USB encryption, keyboard, mouse using 73728 bits. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a CPU that has access to three different security keys based on previous CPU design I have written. I have begun to place a manufacturer label on my Rom Chip please see chart 1 and 2-a.

I would like to thank each and everyone of you for viewing this work !

If you wish to see further work please go to the following website below:

www.barrysscientificbasedproducts.com

www.searchwithbarry.biz

Email bcrouse@protonmail.com

04/11/2023