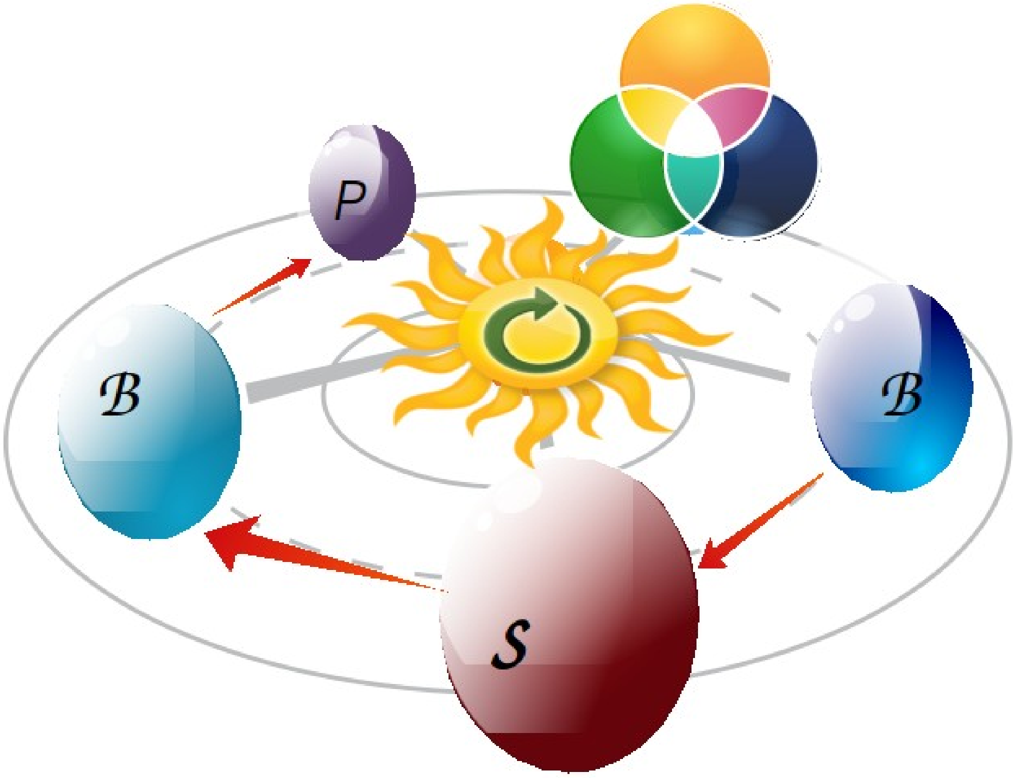

Barrys Scientific Based Products

BARRYS SCIENTIFIC BASED PRODUCTS

Barrys Scientific Based Products BIOS Chip ver 1.2

By

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Introduction

I would like to thank you for taking the time in viewing this work. I have designed and upgraded a BIOS chip that interfaces with the CPU's I have previously designed specifically 128, 256, 384. These CPU's are designed for low end to Middle range servers small to medium level businesses. The new chip Design offers integration with better security approaches taken. The BIOS chip is a 64 pin wire chip titanium plated with the inside using copper wires and built in Ring topology that offers encryption to protect system level based software. The new Bios chip comes with two buffers to process 8192 bits at 128 cycles.. This system is geared more to Linux and Unix based systems.

On a side note, I am introducing my new packaging design on the 1st page. In regards to the new BIOS chip design, I believe that I have developed a new method or process for BIOS based encryption. Chapter 5 presents a short presentation of the Hard Disk and Menu Screen encryption process developed in chapter 4 using 8192 bits.

The Rom chip will continue to go through future updates or revisions. This Rom Chip version has been further developed and upgraded using the BIOS Encryption process that has been designed. I have begun to utilize hard disk encryption on the Chip see chapter on visual design and chapter 5. Future developments will be needed on this chip design

I have updated the menu screen for the BIOS software that will be included in future updates.

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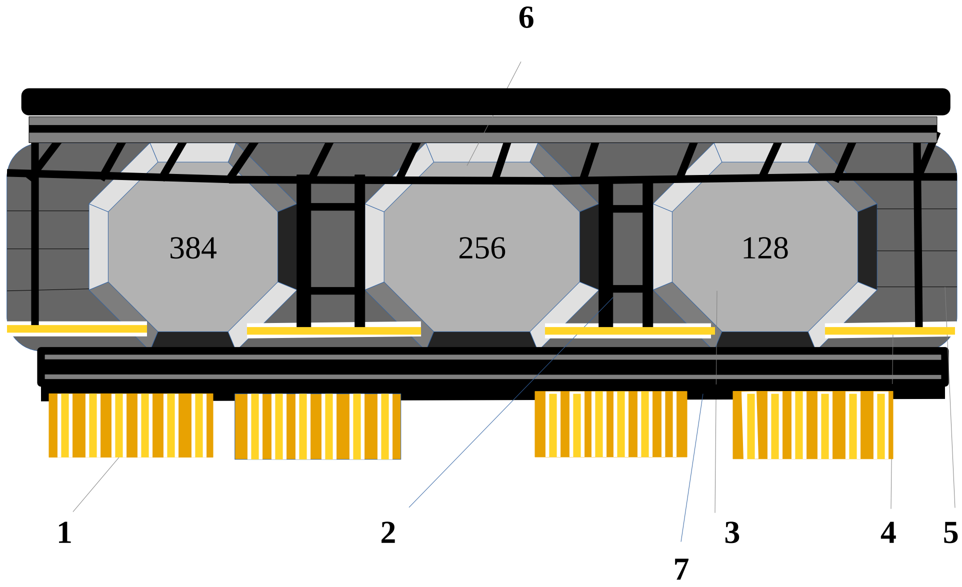
Visual Design

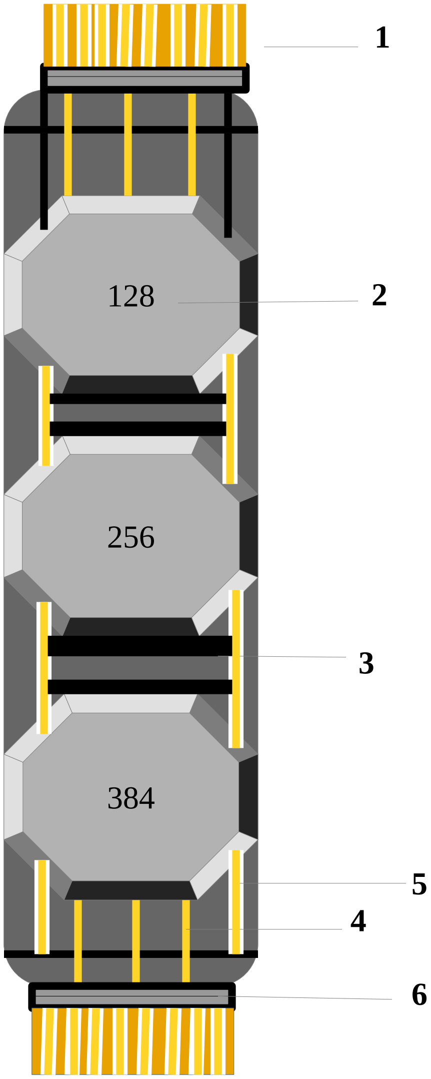
Chapter 1

Visual Chart 1- A BIOS Chip General View



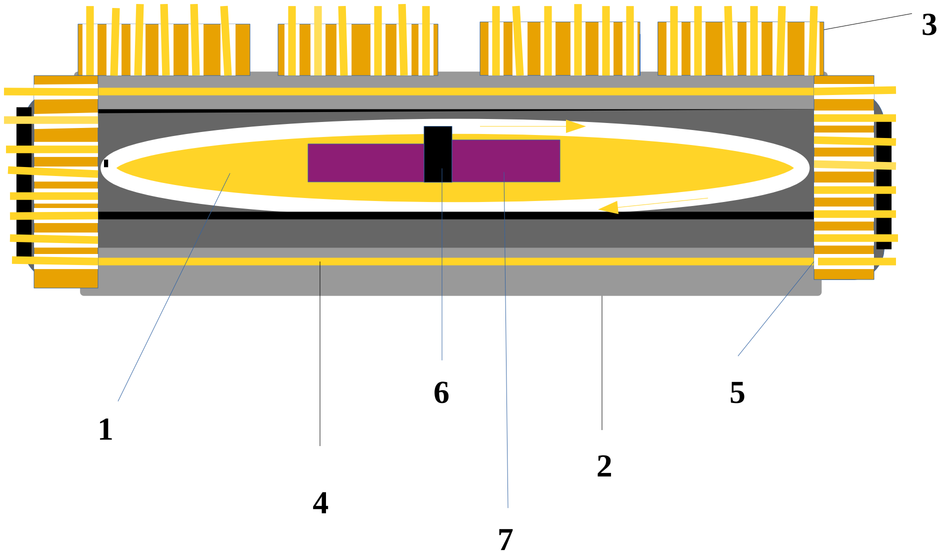
1). 4 banks each bank 6 pins 24 on each side .20 cm white = titanium .10 light gold = copper
2). Switches to 3 CPU's 384, 256, 128 4 total Internal
3). 3 CPU's 384, 256, 128
4). Thick wire .20 Titanium plated .10 copper
5). Thin wire
6). Wire to Pins .10 cm
7). Heat shield

Visual Chart 2- A BIOS Chip Front View



1). Pins 8 on each Side total 16 Pins Titanium white plated .20 cm light gold copper .10 cm
2). 3 CPU’s 128, 256, 384
3). Switches to CPU’s total 4 Internal
4). Thin wire copper .10 cm
5). Thick wire .20 cm titanium plated .10 cm copper
6). wire to Pins

Visual Chart 3- A BIOS Chip front Back View



1). Thick Fiber Optic Ring .20 cm Encryption
2). Back side of Pin touches Thin Fiber Optic
3). Pin Composite White Titanium Plated .20 cm light gold copper .10cm
4). Thin wiring .10 cm
5). Total Pins 64 Vertical 48 pins horizontal 16
6). Data piped to motherboard
7). two buffer area linked to data pipe

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 64 pins 24*2 and 8*2 for each side .The pin composite is .20 cm Titanium plated and .10 cm copper. The front side has 4 wires for a total of 8. Wires on the side are not split. The Bios chip is capable of running the CPU's I previously designed 128, 256, and 384 bits. This allows encryption to take place masking the BIOS and CPU's and now hard disk raided or not. The encryption ring uses .20 cm making thicker wires to push more bits through.

The BIOS chip also has Thin wires that are copper plated .10 cm non titanium plated along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches.

On the back side of the BIOS chip see chart 3-A has a thick fiber optic ring network topology and two buffers with a way to pipe more bits to the mother board and uses I/O Scheduling allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption process and or method

Encryption method for Password

BIOS Pins	# Cycles	CPU used	padded bits
64	8	128	384
64	16	256	768
64	24	384	1152

Equation Equals BIOS Pins * Number of cycles minus CPU

BIOS Pins	#CPU	Password field length	Bit Strength
64	128	8	512
64	256	16	1024
64	384	24	1536

Equation is CPU add padded bits/64 equals password length = Bit Strength

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 128 Padded Bits 384 / 64 equal 8 characters for my security key because I am allowed 64 characters I can than pad the other 56 characters for my security key thus my security key would look like this below:

56 Characters padded random number generated burned into chip

25905698xxxxxxxxxxxxxxxxxxxx equals 64

8 character

If I took 256 plus 1024 / 64 I could use 20 characters and 44 characters padding also 384 plus 1152 /64 equals 24 Characters with 40 character padding. **This is a example of only 1 cycle if you turn to the next page I use 8 cycles for my process.**

Real Characters	**Padded Characters**	**Constant 64**
8	56	64
20	44	64
24	40	64

Security Key Encryption

CPU	Constant = 64 bits	#Characters	Character pad
128	64	16	48
256	64	32	32
384	64	48	16

Equation = 1). CPU*8 /64 = #Characters

A = 64

2). A – Character Representation = Character Padding

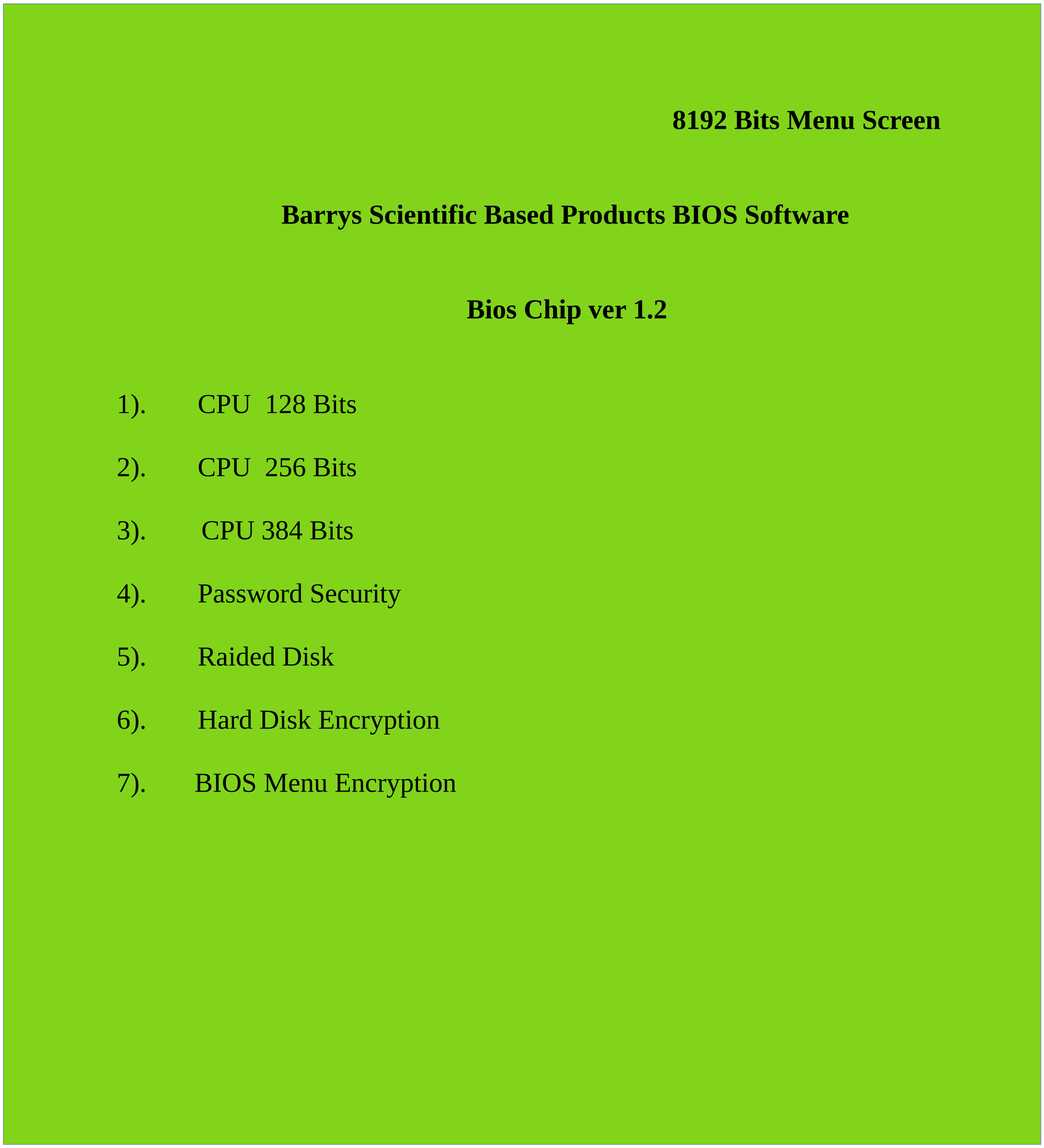
This idea would create 3 security keys used for each CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key 64 equals Password Length 64

Each security key is different and unique depending on the CPU used. The Equation takes a CPU multi ply by eights divide by 64. The 2nd step is declare A =64. The 3rd step is A – Character representation gives you the amount of padding you can use which represents character representation. because I am allowed a total of 64 characters using the method and adding the padding I can now extend my security keys to 64 characters.

Chapter 4

Menu Screen



8192 Bits Menu Screen

Barrys Scientific Based Products BIOS Software

Bios Chip ver 1.2

1). CPU 128 Bits

2). CPU 256 Bits

3). CPU 384 Bits

4). Password Security

5). Raided Disk

6). Hard Disk Encryption

7). BIOS Menu Encryption

Chapter 5

Hard Disk Encryption

After reviewing Chart 3-a, I can now create Hard Disk and Menu Screen Encryption because I have a BIOS chip that has a builtin Network Topology Hardware and System level software based on the following parameters:

1). Bios Pins 64 Pins
2). assigned variable 8192 Bits

The Equation is 8192 bits / 64 = 128 cycles based on the hardware using thick wires it would take 128 cycles to encrypt the hard disk. This would create bottle necks. The solution is to create two area buffers to load the cycles into the Data Pipe meaning each buffer could load 64 cycles since there are two and would equal 128 cycles. This would alleviate bottle necks by using the I/O scheduling mechanisms for each buffer.

Chapter 6

Final Thoughts

The Bios chip is designed for low end to Middle range servers using 128, 256, and 384 Bit CPU’s previously designed for small and middle range businesses.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it’s number of bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is now using a mathematical process and or method working with 64 bits. I have updated the Menu Screen using this BIOS chip at 8192 bits encrypted.

The BIOS chip uses 64 pins with the backside of the chip using a thicker internal fiber optic ring topology that utilizes encryption to protect the BIOS software. I have created two buffer areas that would allow for hard disk encryption using 8192 bits. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a selection of 3 different CPU’s as a selection based on previous CPU designs I have written.

I would like to thank each and everyone of you for viewing this work !

If you wish to see further work please go to the following website below:

www.barrysscientificbasedproducts.com

Email bcrouse@protonmail.com

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