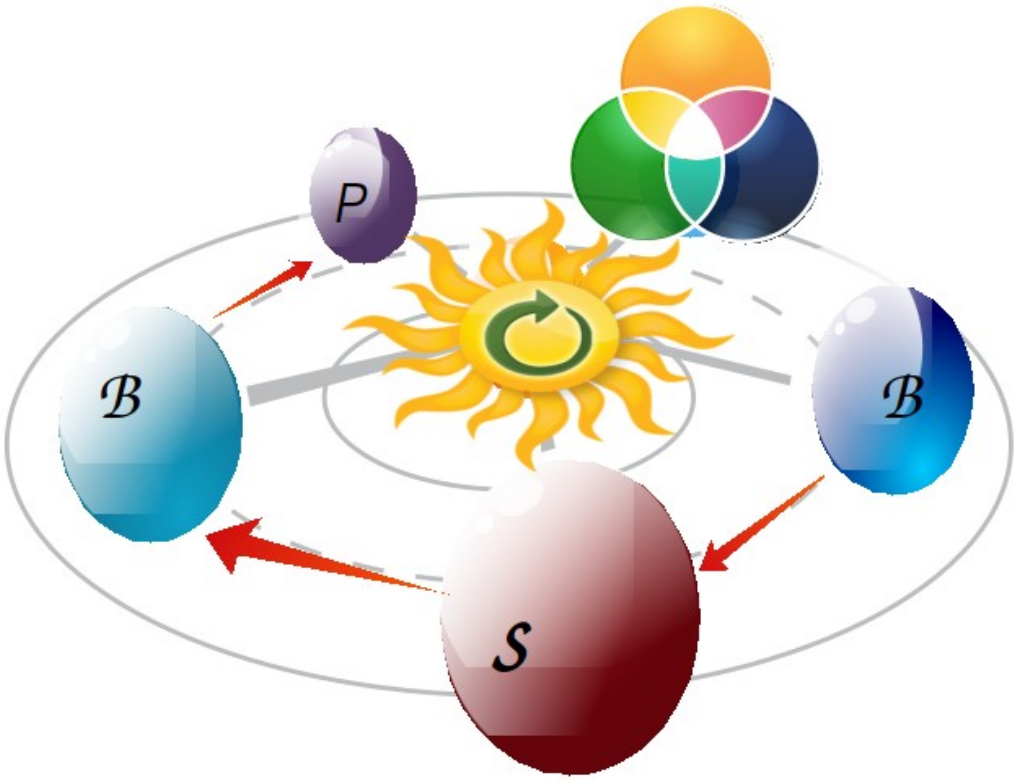

Barrys Scientific Based Products

Barrys Scientific Based Products BIOS Chip ver 1.0

By

Barry L. Crouse

Introduction

I would like to thank you for taking the time in viewing this work. I have designed a BIOS chip that interfaces with the CPU's I have previously designed specifically 128, 256, 384. These CPU's are designed for low end Middle range servers small to medium level businesses. The chip Design offers integration with better security approaches taken. The BIOS chip is a 32 pin wire chip with a built in Ring topology that offers encryption to protect system level based software. The chip has built inside 3 objects that are used for the CPU's as mentioned above. This system is geared more to Linux and Unix based systems.

On a side note, I am introducing my packaging design 1st page used on this work.

The Rom chip will have to go through some updates or revisions. This Rom Chip version presents a basic foundation for future updates and revisions.

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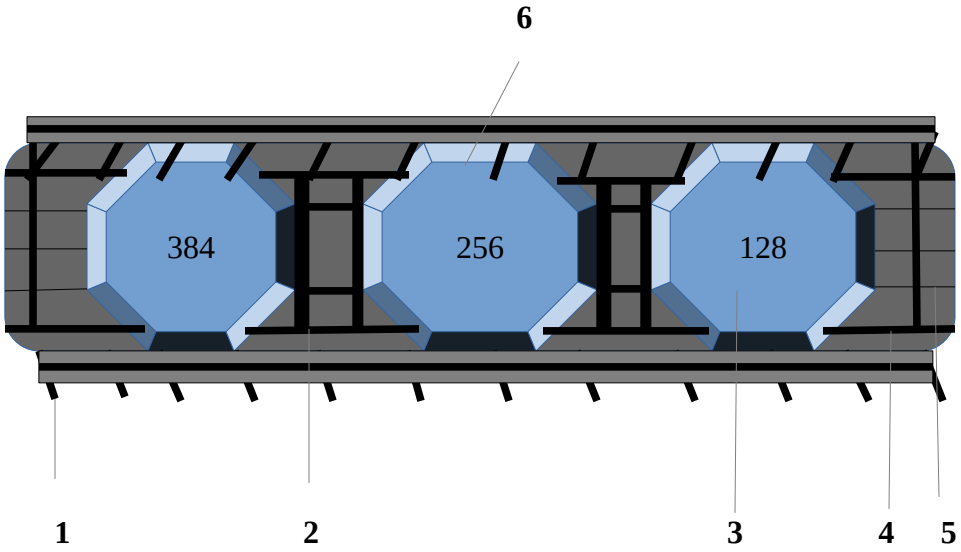
Visual Design

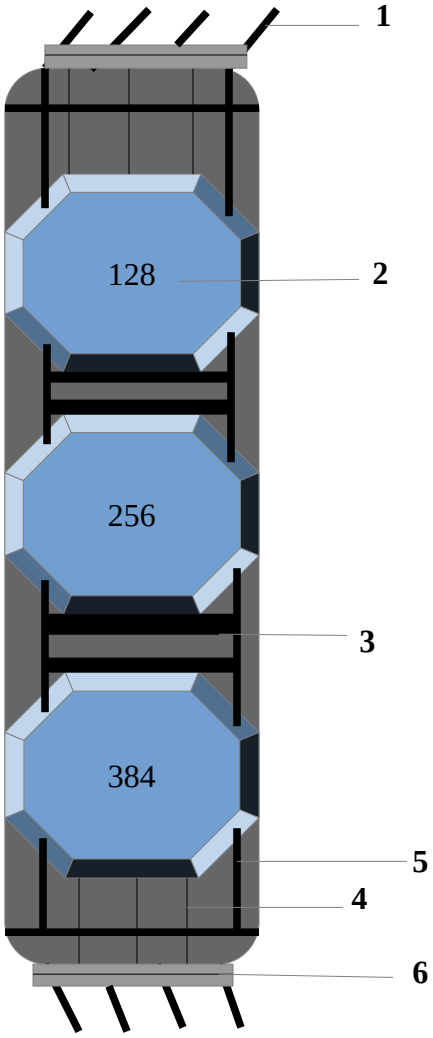
Chapter 1

Visual Chart 1- A BIOS Chip General View



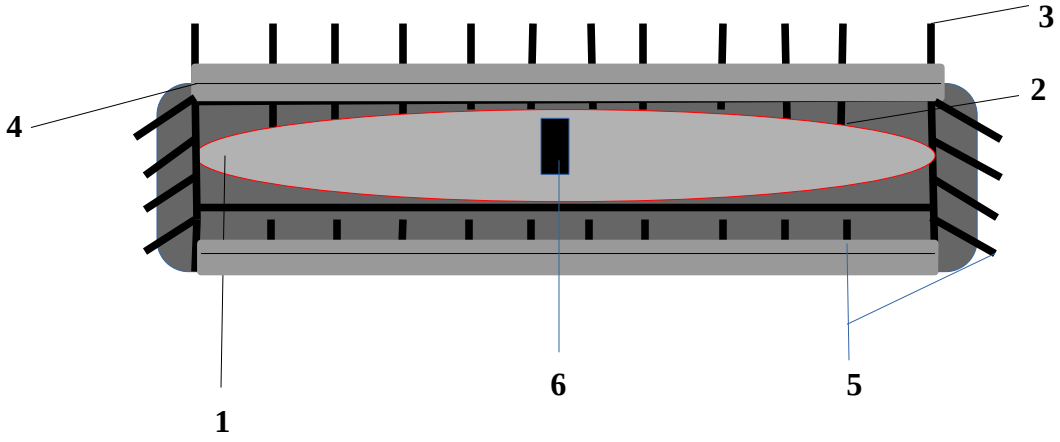
1). Pins to chip 12 on Each side total 24 pins .10 cm
2). Switches to 3 CPU's 384, 256, 128 4 total Internal
3). 3 CPU's 384, 256, 128
4). Thick wire .10 cm
5). Thin wire
6). Wire to Pins .10 cm

Visual Chart 2- A BIOS Chip Front View



1). **Front side Pins 4 on each Side total 8 Pins**
2). **3 CPU's 128, 256, 384**
3). **Switches to CPU's total 4 Internal**
4). **Thin wire**
5). **Thick wire .10 cm**
6). **wire to Pins**

Visual Chart 3- A BIOS Chip Back View



1). Thin Fiber Optic Ring Encryption
2). Back side of Pin touches Thin Fiber Optic
3). Front Side of Pin
4). Thin wiring
5). Total Pins 32
6). Data piped to motherboard

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 32 wires 12 on each side for a total of 24. The front side has 4 wires for a total of 8. The Bios chip is capable of running the CPU's I previously designed 128, 256, and 384 bits. This allows encryption to take place masking the BIOS and CPU's.

The BIOS chip has Thick wires .10 cm and thin wires along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches.

On the back side of the BIOS chip see chart 3-A has a thin fiber optic ring network topology with a way to pipe more bits to the mother board allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption methods

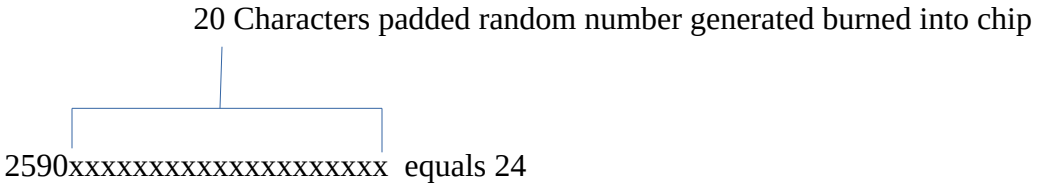
Encryption method for Password

BIOS Pins	# Cycles	CPU used
32	4	128
32	8	256
32	12	384

BIOS Pins	#CPU	Password field length	Bit Strength
32	128	24	3072
32	256	32	8192
32	384	32	12288

The Equation is Bit strength / CPU equals password length.

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 128 / 32 equal 4 characters for my security key because I am allowed 24 characters I can than pad the other 20 characters for my security key thus my security key would look like this below:



If I took 256 / 32 I could use 8 characters and 24 characters padded also 384/32 equals 12 Characters with 20 padded. Please see on next page.

Security Key Encryption

CPU	Constant = 32 bits	#Characters	Character pad
128	**32**	**4**	**20**
256	**32**	**8**	**24**
384	**32**	**12**	**20**

This idea would create 3 security keys used for each CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key equals Password Length

Each security key is different and unique depending on the CPU used. I will now present my final thoughts in the next chapter.

Chapter 4

Final Thoughts

The Bios chip is designed for low end Middle range servers using 128, 256, and 384 Bit CPU's basically designed for small and middle range businesses.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it's number of bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is not built using a mathematical process but rather based on random number selection for the padding scheme to match the password field length.

The BIOS chip uses 32 pins with the backside of the chip using a internal fiber optic ring topology that utilizes encryption to protect the BIOS software. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a selection of 3 different CPU's as a selection based on previous CPU designs I have written.

I would like to thank each and everyone of you for viewing this work !

If you wish to see further work please go to the following website below:

www.barrysscientificbasedproducts.com

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12/23/2022

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