Barrys SS-95 Motherboard Design

by

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Introduction

I would like to take the time in Thanking each and everyone of you for reading this Science and technology based work. I have made improvements on the SS-95 Motherboard Design please view the following modifications:

a). Dual Core memory chip
b). Dual Core CPU with Dual Pipe and added area of space for CPU 2
c). Dual BIOS fault tolerance and Integrity
d). New Geometric Design fitting for Internal and External Connectors
e). Video Card updated with area of space security
f). New Internal hardware ROM Chip geometric Design with 16384 bits

1). The Visual **Model Super Sonic 95 Motherboard 1-A General View** overall view of the product and demonstrates a Industrial Design because of it's unique characteristics. The detailed features that are within the Design accompanies in views 2-a through 9-A with detailed specs. The features of this design comes with a CPU that can make path choices either using 3 thin wires or 2 thick wire to access each CPU based on Intelligent Design paths Design Patent application.

2). **Patent Ideal 2 Method and Single 32768 Data Block processing. T**his is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself and is upgraded as well.

3). **Patent Idea 3 New Cryptographic Energy Model Design.** This is shown as an Industrial Design along with the method and process. This comes with dynamic bit data strings, linear and dual curvature elliptic circles with password encryption and padding Mathematical equation with process and method.

4). **Patent idea 4 Video Card** I have updated the Video card and slot with 4 areas of space using PKCS 12 security for each area of space key and sub key promoting security and privacy when viewing within the structure of this IT hardware motherboard.

a). PKCS 12 = 1 area of space 8192 bits = 4 areas of space * 8192 = 32768 total bits

This is a 3rd generation motherboard Design. Once again thank you for reading this work !

5). **New Dual Core memory chips**

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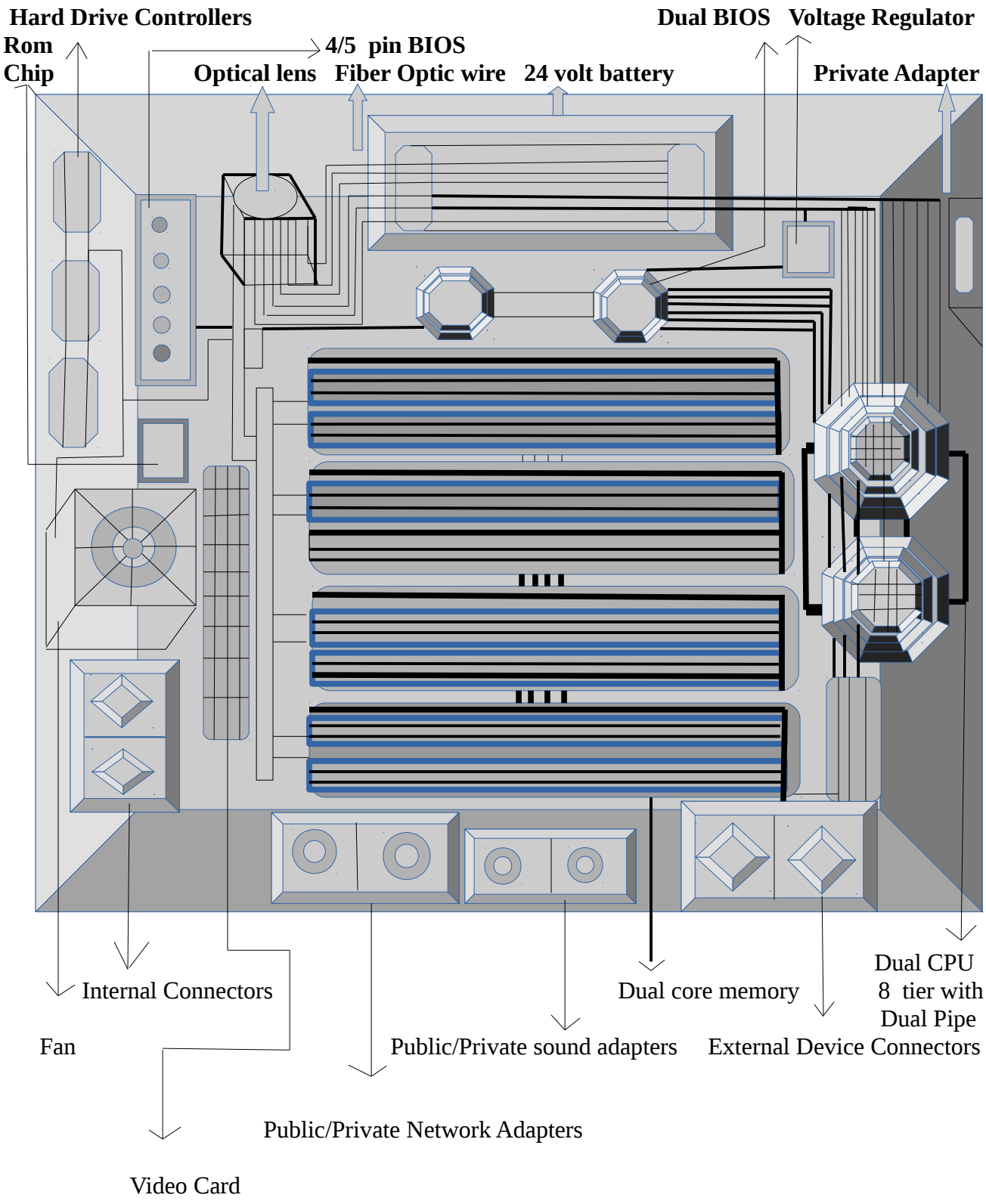
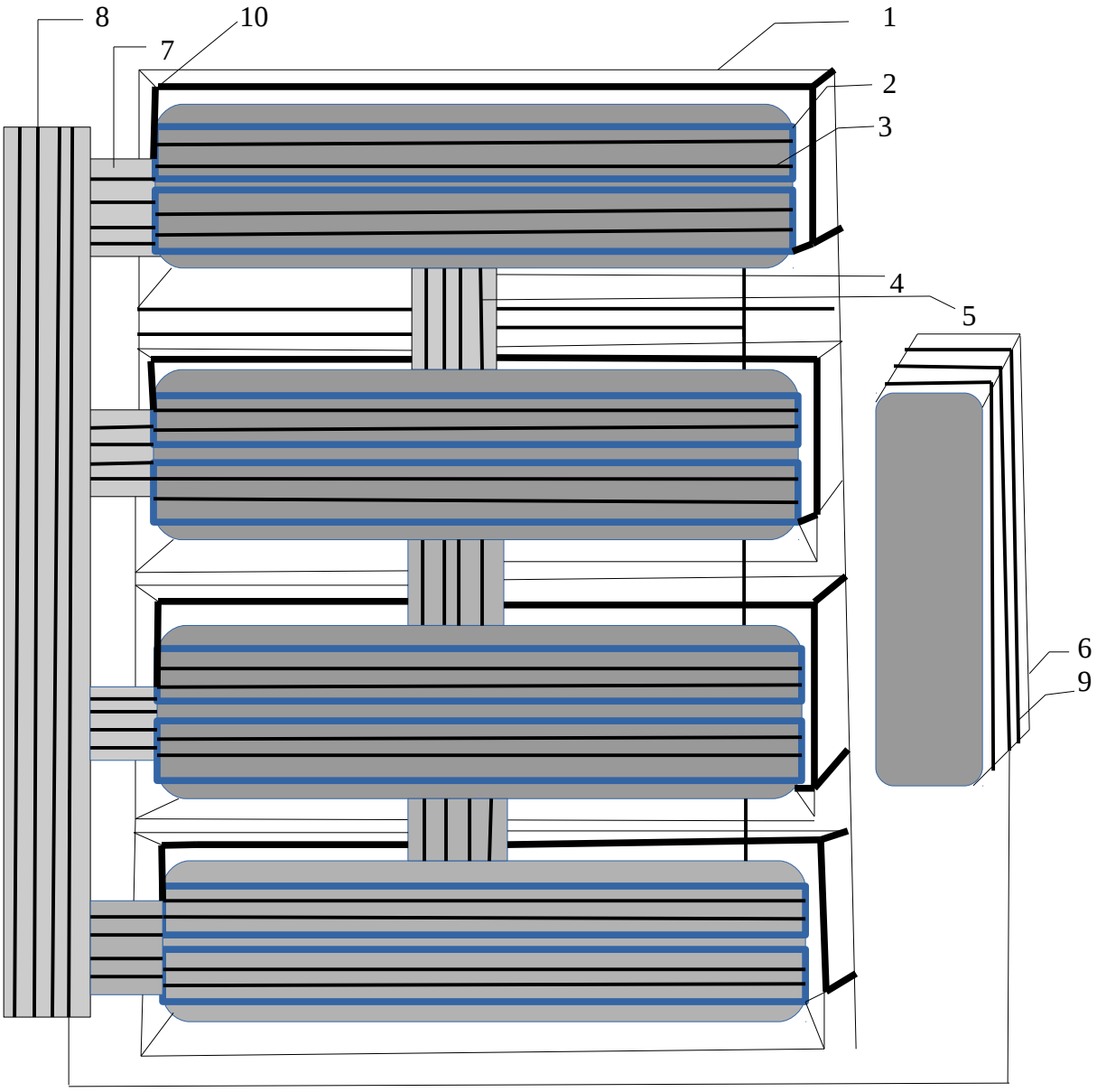
Model Super Sonic 95 Motherboard- Design 1-A General View



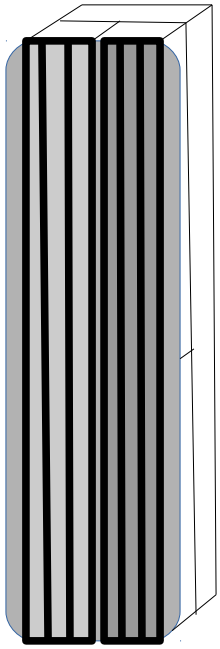
Model Super Sonic 95 Dual memory Core General View 2-A



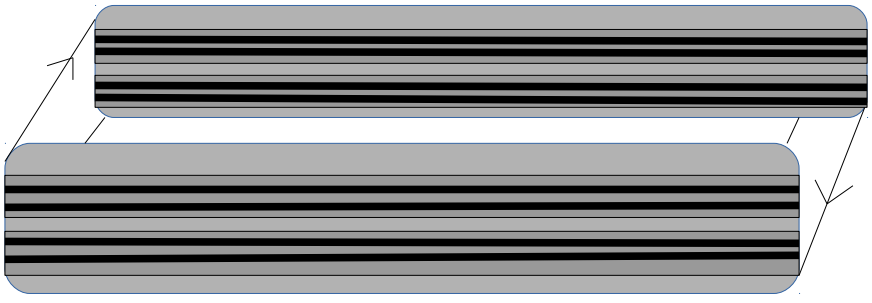
1). Fitting to hold Memory Chips
2). Banks 4 banks per Dual Core memory chip total 8 2048 per bank total 4096 bit addressing scheme
3). Data Strings 4 strings per Bank 2048 bits per string total 8 strings per chip 4096 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 1024 bits per wire total 4096 bits
6). Reserved Memory area (Buffer) 3072 bits
7). Fiber Optic tube address encasement
8). Address Bridge 4 wires 1024 bits per wire to process Fiber Optic
9). three Data wires for holding in reserved space 1024 per wire
10 Dual Core Memory Chips

Model Super Sonic 95 Motherboard memory Front and Side View 2-A

Dual Core

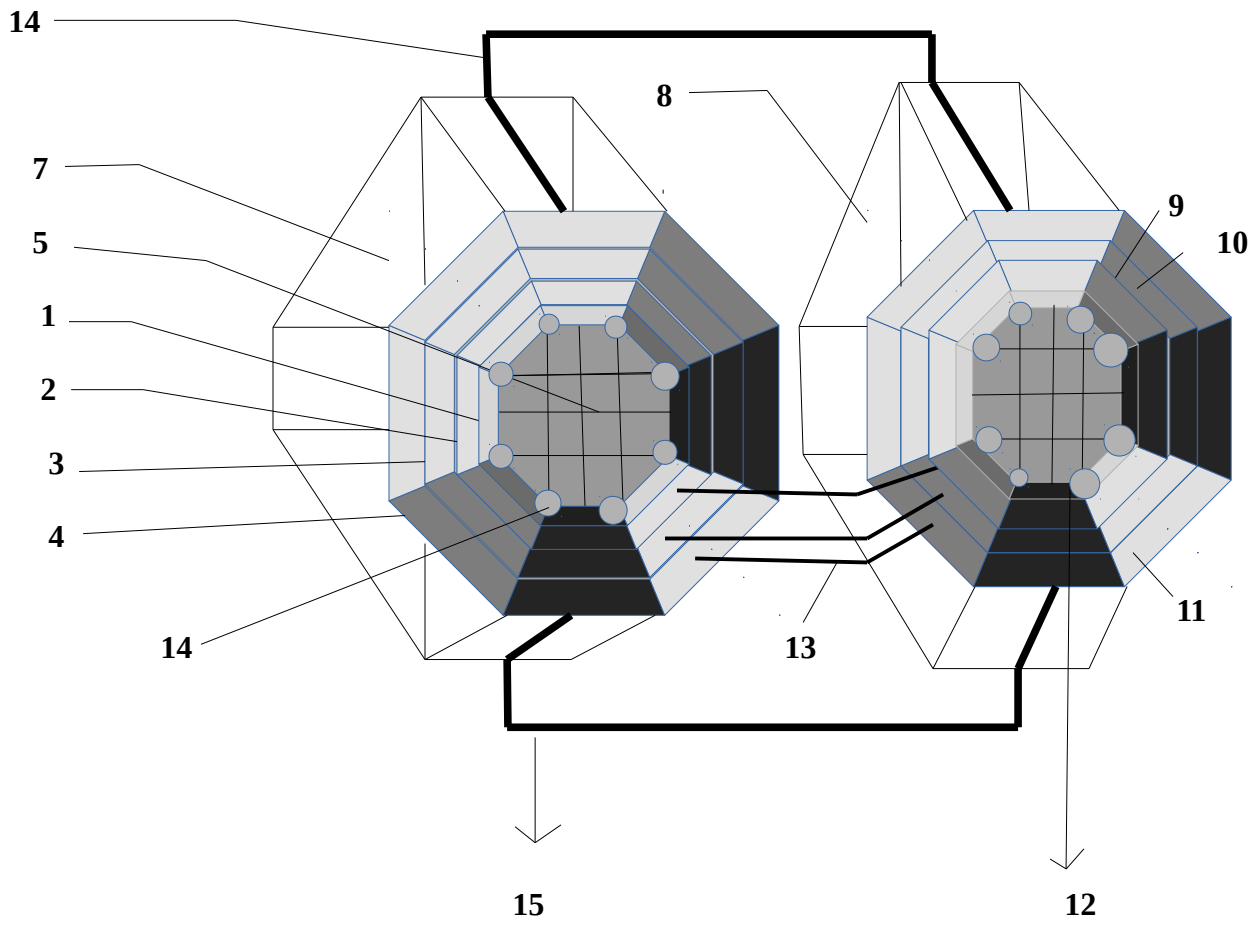


Dual Core Memory Front View



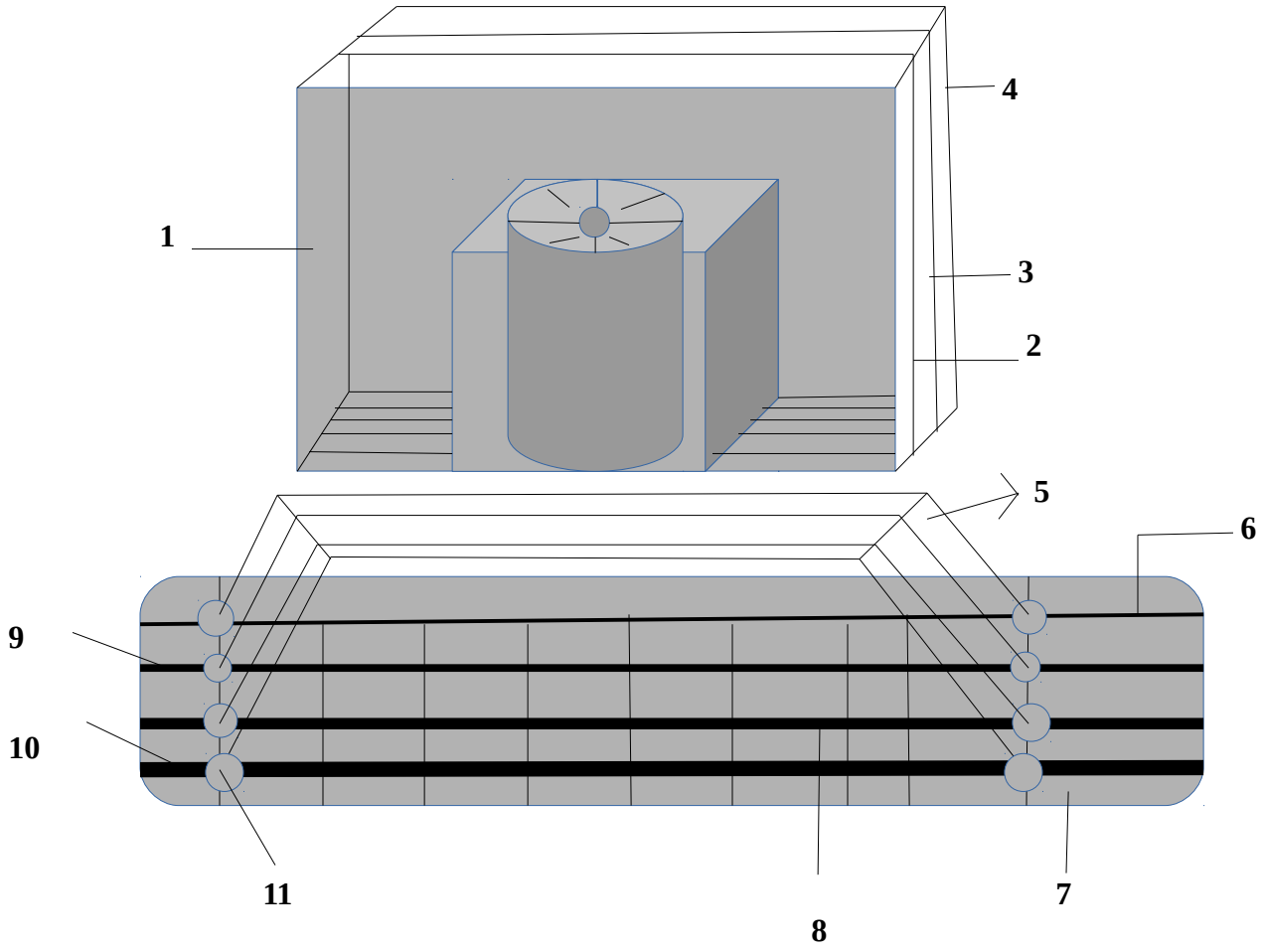
Dual Core Memory Side View

Model Super Sonic 95 Industrial Dual Core CPU Idea 3-A



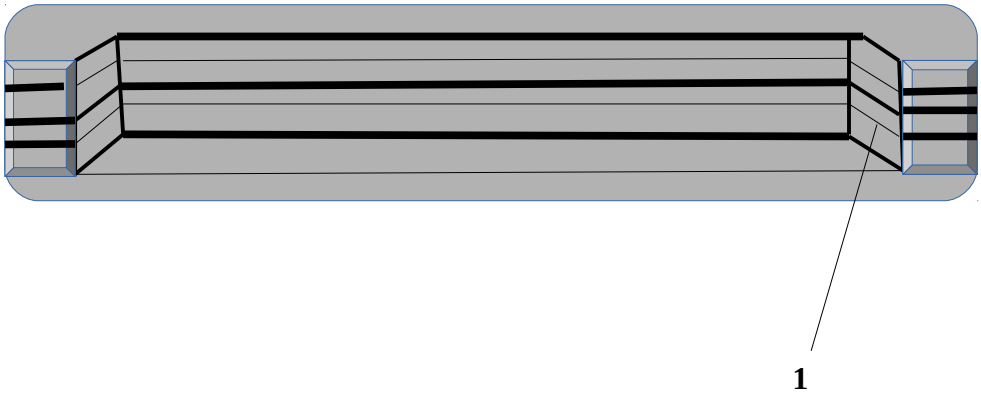
1). Public CPU 1 Area of Space 4096 Bits CPU 1
2). Private CPU 1 Area of Space 4096 Bits CPU1
3). Shared CPU 1 Area of Space 4096 CPU1
4). Reserved CPU 1 Area of Space 4096 Bits CPU1
5). Fiber Optic Net
6). CPU Fitting
7). CPU 1
8). CPU2
9). CPU 2 Public Area of space 4096 bits for CPU 1
10). CPU 2 Private Area of space 4096 for CPU 1 and CPU2
11). CPU 2 Shared CPU Area of Space 4096 bits for CPU 2
12). CPU 2 Reserved CPU 2 Area of Space 4096 CPU2
13). 3 thin Wires connecting CPU 1 and CPU 2
14). Gateway Node Points
14). Alternate dual Pipe Wiring path 1 Thick Wiring
15). Alternate dual Pipe Wiring path 2 Thick Wiring

Model Super Sonic 95 Industrial Fan Idea 4- A General View



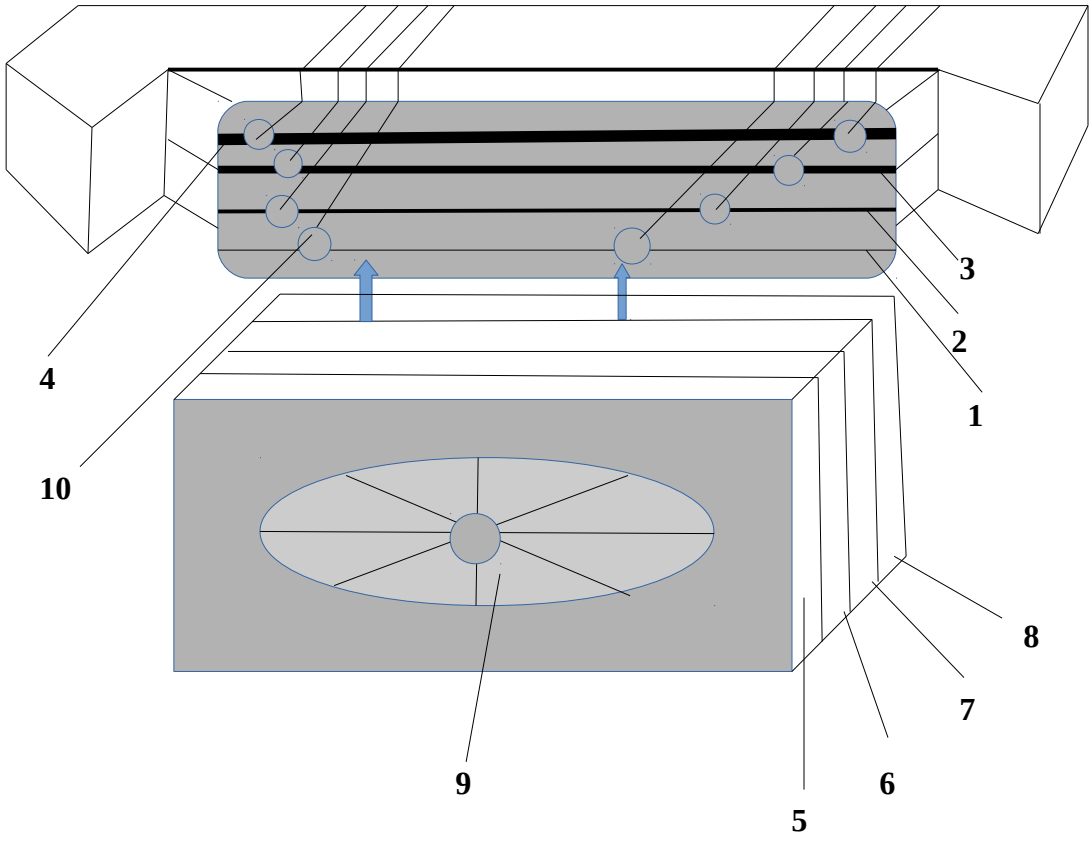
1). Public Video Area Space PKCS12 8192 4096 bit key and 4096 sub key
2). Private Video Area Space PKCS12 8192 4096 bit key and 4096 sub key
3). Shared Video Area Space PKCS 12 8192 4096 bit key and 4096 sub key
4). Reserved Video Area Space PKCS12 8192 4096 bit key and 4096 sub key
5). Video Data Bride 4 slots
6). Public Data String
7). Titanium video fitting
8). Shared Data String
9). Private Data String
10). Reserved Data String
11). Node Points (End to End point connection)

Model Super Sonic 95 Industrial Patent video slot 5-A General View



1) **Side view of the slot where the Video Card is placed.**

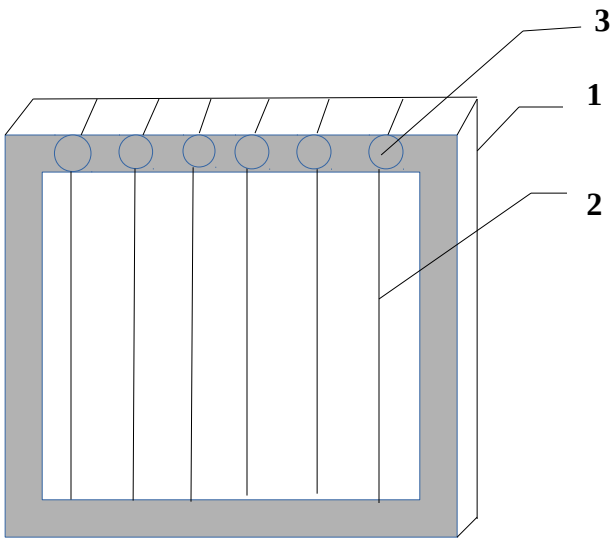
Model Super Sonic 95 Industrial Video slot specs Idea 6-A General View



1	**Public Data String with 8192 pkcs12 4096 key and 4096 sub key**
2	**Private Data String with 8192 pkcs12 4096 key and 4096 sub key**
3	**Shared Data String with 8192 pkcs 12 4096 key and 4096 sub key**
4	**Reserved Data String with 8192 pkcs12 4096 key and 4096 sub key**
5	**Public Video Slot**
6	**Private Video Slot**
7	**Shared Video Slot**
8	**Reserved Video Slot**
9	**Video Fan**
10	**Node Points**

Model Super Sonic 95 Industrial Idea 7-A General View

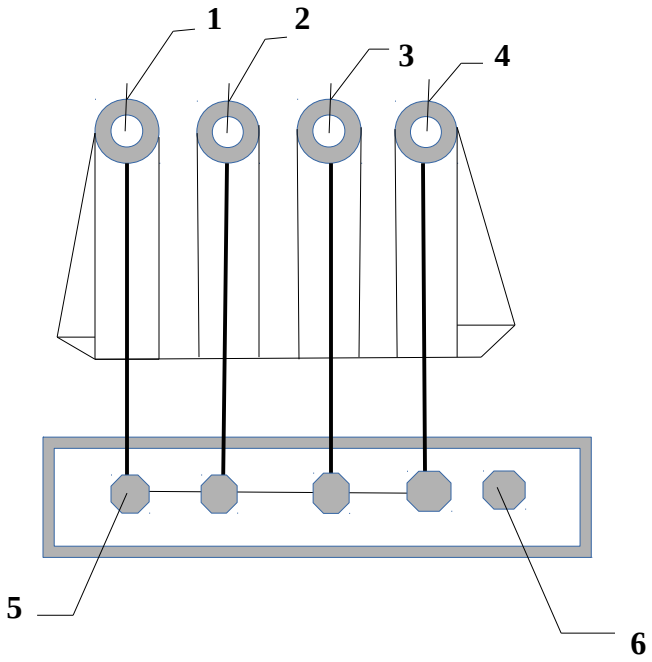
Voltage Regulator 5 wire Check



1). Overall view of chip
2). 6 wires inside chip to check flow of voltage 1024 bits per wire total 6144 bits
3). Node Point check testing wires for on and off conditions

Model Super Sonic 95 Industrial BIOS Idea 8-A General View

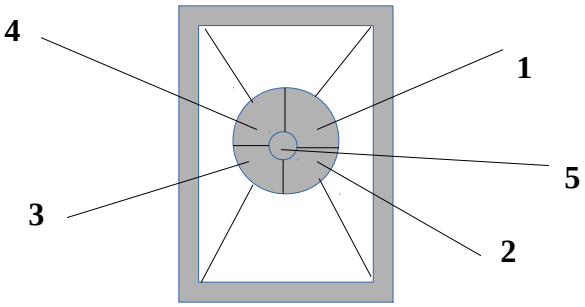
4/5 Pins BIOS



1). Public BIOS Pin
2). Private BIOS Pin
3). Shared BIOS Pin
4). Reserved BIOS Pin
5). BIOS Bins that connect to node Points
6). BIOS Pin Clearing areas of spaces

Model Super Sonic 95 Industrial ROM Chip Idea 9-A General View

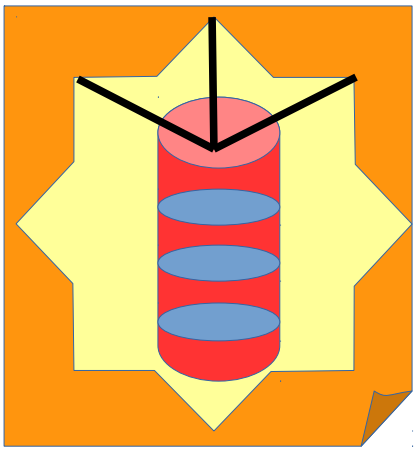
16384 Built in Certificate ROM Chip



1). Public Area of Space
2). Private Area of Space
3). Shared Area of Space
4). Reserved Area of Space
5). Certificate on burned on platter read only

Model Super Sonic 95 Industrial Rom Chip specs Idea 10-A General View

Barrys Scientific Based Products 16384 Bit Hardware Verification Certificate



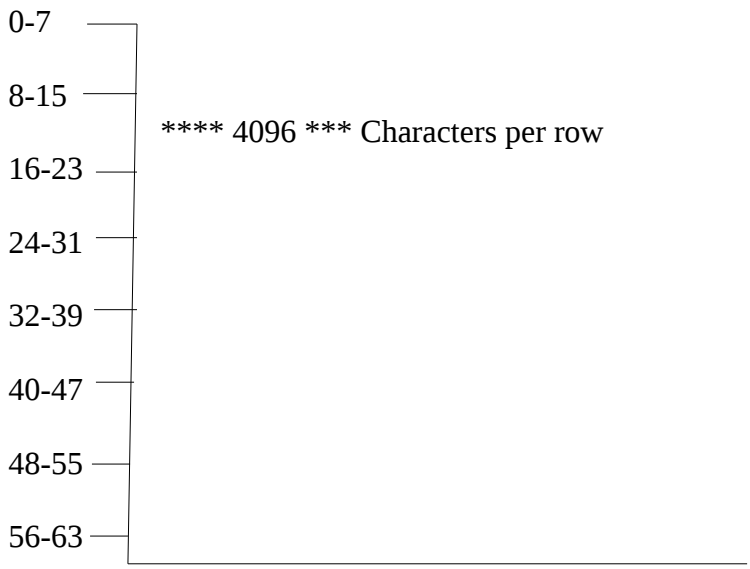
This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip.

1). RSA Sign Only 4096
2). RSA Encrypt 3 sub keys 12288

Chapter 2

Single 32768 Data Block processing

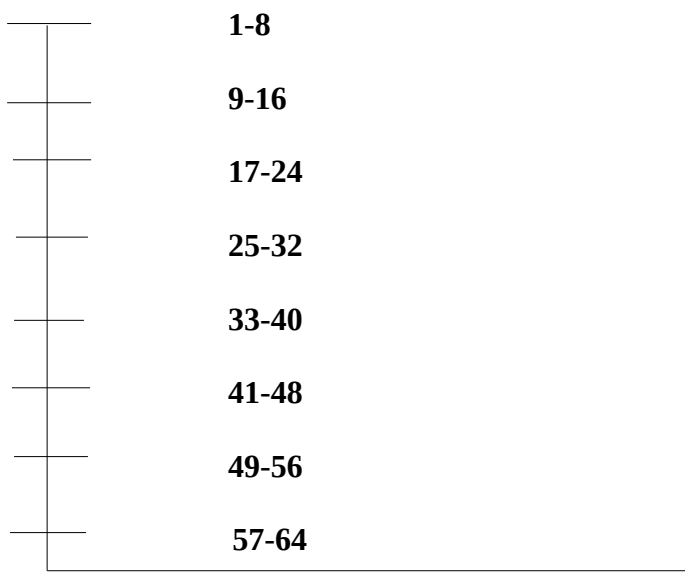
I will begin by defining the block data of 4096 characters with the 2048 bit addressing scheme from here I will create a matrix of 6 rows each with 4096 characters matrix. See chart below. I am going over the method and process defined below.



4096 * 8 rows = 32768 bits

Since I have defined my address scheme as 2048 bits. I divide 32768 by 2048 bits and it comes up with 16 frames. I divide 16 frames by 2 = 8 frames * 4096 byte frames in bursts equals 32768. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 0 and 1. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create eight packets of 4096 byte frames equal to 32768 I can take this further by demanding each packet is authenticated with a 16384 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame’s of 62 and 63 with final packet assembly reaching the end point of communication.

Packet #	Frame sequence
1	**1-8**
2	**9-16**
3	**17-24**
4	**25-32**
5	**33-40**
6	**41-48**
7	**49-56**
8	**57-64**



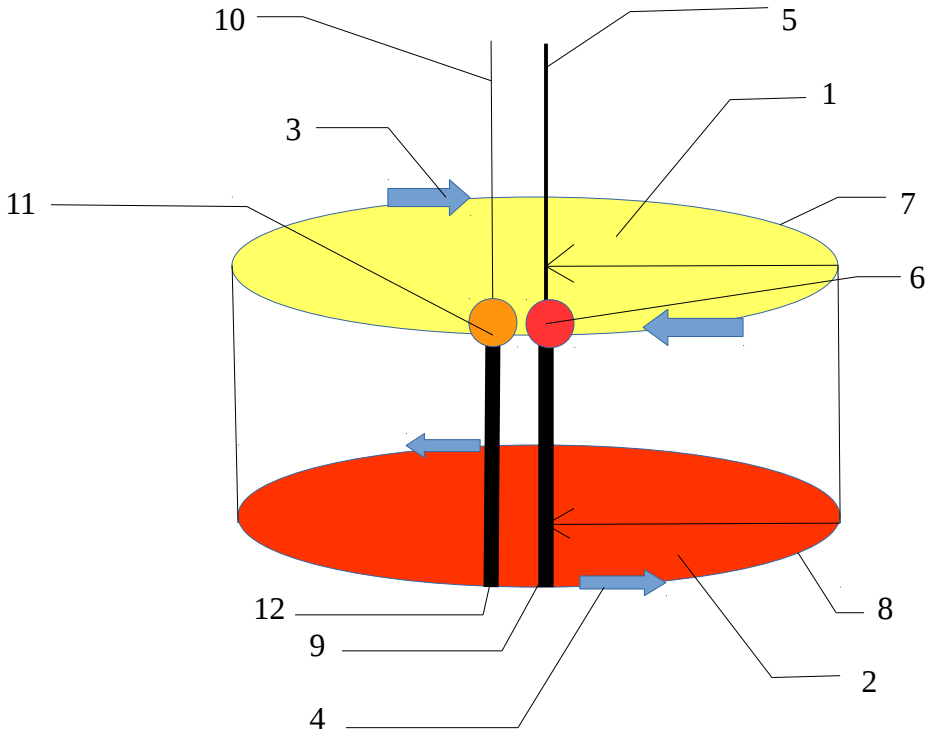
4 packets of 4096 bytes burst with frame sequences of 8.

1). 32768 / 8 = 4096 Frames of 8
2). 512 per frame sequence = 8 * 512 = 4096

Chapter 3

New Cryptographic Energy Model Design

Cryptographic Energy Model Visual Design



1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. 1st Data String a 768 bits a
6. Gateway Check node point 1st dimension
7. yellow Elliptic curve 953 Bits
8. Orange Elliptic Curve 967 Bits
9. 2nd Data String a 1280 Bits
10 1st Data String b 512 Bits 2nd Dimension
11 Gateway Checkpoint 2nd Dimension
12 2nd Data String b 1024 Bits

Cryptographic Energy Model Design Method and Process

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B curvature is represented by shades of yellow and orange -color spectrum's. The 1st curvature uses 953 bits and the 2nd uses 967 for a total of 1920 bits. Depending on the number of cycles used examples 9 and 11 I can generate 953 * 11 = 10483 bits + 967 * 13 = 12571 bits total bits. 23054 < 32768 The system architecture can only support 32768 bits so the number of cycles could support asymmetrical cycles 11 and 13. To complete the processing I must now add the linear strings of the following

1st data string a = 768
1st data string b = 512
2nd data string a = 1280
2nd data string b = 1024

data array = 23054 (elliptic) + 768 + 512 + 1280 + 1024 (linear) = 3584 this system supports this model because 26638 < 32768

The Cryptographic models are based on the Color spectrum's when crossing to dimensional space in relations to linear based strings. The Elliptic colors use more heat and energy as well.

If I set up a series of arrays we could find the total number of bits based on the following example above

1st Curvature = a
2nd Curvature = b
1st data string = c
2nd data string =d
a= 10483
rem 1st curvature 953 *11 cycles

b= 12571
rem 2nd curvature 967 * 13 cycles
c = 768
d = 512
e= 1280
f = 1024

array-1 = {a,b}
rem curvature
array-2 = {c,d,e,f}
rem linear
array-3 = array-1 + array-2
array-3 =23054+3584 = 26638 bits

This system design could support this Cryptographic model because 26638 < 32768 bits

This model uses a combination of both Linear and Curvature motion and Color spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon.

I can now subtract 32768 – 26638 and now have =6130 bits to use for my password encryption.

This model uses a combination of both Linear and Curvature motion and Color Spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 6130 bits I could also create a cryptographic password that insures each IP Packet Integrity and authenticity example:

1). I can use a Data string of 512 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 929 bits with 6 cycles= 5574 bits. The next step is to add the 512 bits = 6086 bits to use for password security. The Equation can be written as follows:

Z {p1+,P2-} = 512 bits Linear

Y = 5574 bits= Curvature

W = Z + Y

B = W/1
B= W/3

I have created two spaces that can be used to break 4647 bits into chunks of data this creates a mechanism for multiple paths the final product is below:

B = 6086/1 = 6086
B = 6086/2 = 3043

To reverse this you simply take the final product * the number being divided example:

3043 * 2 = 6086

If you will notice, I have 44 bits left over, This needs to be utilized and how this can be used is by padding the password encryption with the spare bits. This can be achieved by the following:

6130 – 6086 = 44 bits

B =6086/1 =6086 + 44 Bits

B = 6086/2 = {3043 + 22}1st subscript + {3043+22}2nd subscript total = 6130 . Thus I have created double subscript for password and padding a IP packet that needs protection. If I want to add extra protection for each subscript simply compress the script

{3043+22 = √3065 = 55.362442143 1st subscript the 2nd subscript I would not want to compress it because of the principles of asymmetry not balanced form of energy. I could even choose whether to compress subscript 1 or 2 making it even harder because the worst thing a adversary can do is guess.

The equation could be written as such $(\sqrt{a \text{ or } b})+ c = d$

You can either compress a or b than add the constant which in this case is 3065 of course to reverse the compression you can square root (55.362442143) 2nd power demonstrating the principles of reverse mechanics.

I will now write my final thoughts on this Projects

Final Thoughts

Chapter 4

I have improved upon my CPU Model by using Alternate Path usage. The CPU can have the ability to make choices that is best suited for processing example The CPU can take the 1st choice of accessing the three thin wires or the other choice using either or two thick wires depending on the metrics of throughput usages.

This project involved making improvements on prior existing designs along with modifications. I also created a password algorithm for this project along with padding also created subscripts used for padding the address spaces creating a extra layer of IP packet protection along with password protection.

I have updated the Video card to provide some level of privacy and security using PKCS12 8192 bits per area 4096 bit keys and 4096 bit sub keys total 4 areas of space * 8192 bits = 32768 bits. This can be done creating 8192 PKCS12 Certificates and has been proven by creating a self signed certificate recently in the summer of 2018.

I also updated the Cryptographic model with dynamic linear strings and dual curvature blocks also I have created a built in 16384 ROM certificate 1 RSA sign and 3 sub keys demonstrating principles of Dynamic Energy being deployed.

I have reached the outer limits of this type of design and specifications without a major overhaul which may in the future introduce a 4th generation of motherboard Designs.

This work is in memory of my Dad Leon Crouse who died on 12/07/2018

If you wish to view more work, Please visit my website below

www.barrysscientificbasedproducts.info

Email crouseb395@gmail.com

01/07/2019

Barry L. Crouse