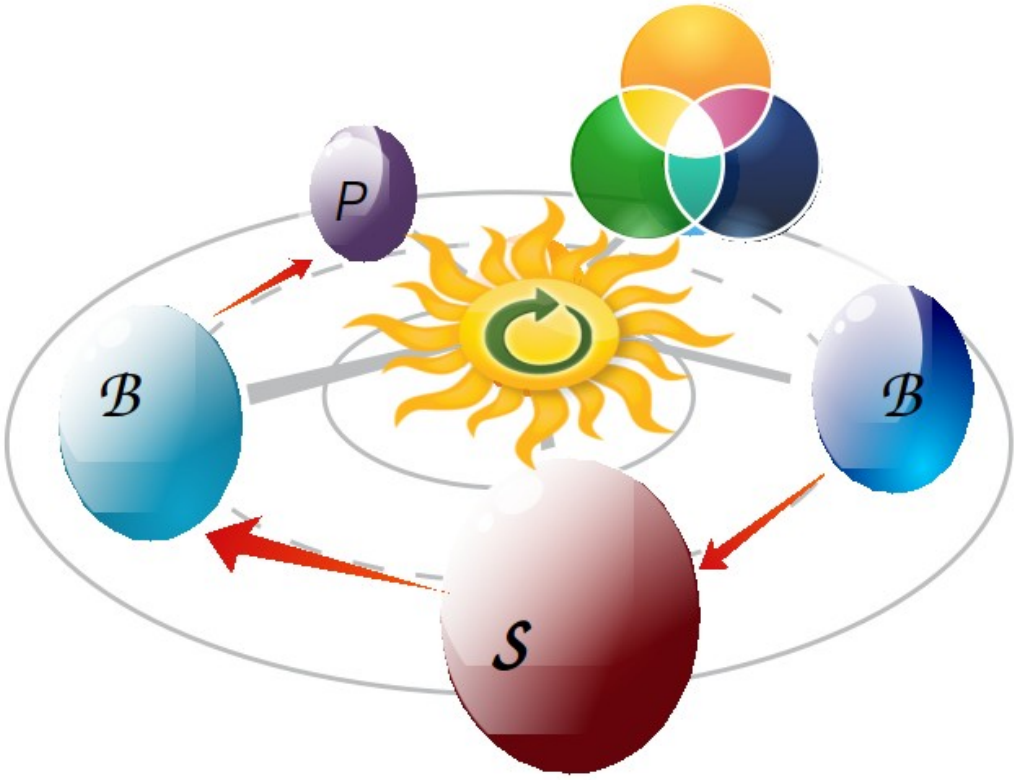


Barrys Scientific Based Products

Barrys Scientific Based Products BIOS Chip ver 1.5

By

Barry L. Crouse

Introduction

I would like to thank you for taking the time in viewing this work. I have upgraded and improved this BIOS chip that interfaces with the CPU I have previously designed specifically 648. The CPU 648 is designed for middle range servers medium level businesses. The new chip Design offers integration with better security approaches taken. The BIOS chip is a 648 pin wire chip titanium plated with the inside using copper wires and built in Ring topology that offers encryption to protect system level based software. Please be aware that the pins are dual sided similar to server side memory chips. The new Bios chip comes with four buffers to process 88128 bits at 136 cycles. This system is geared more to Linux and Unix based systems. I have added thin wires for the usage of tunnelling protocols also tunnelling protocols have been added to the menu screen This new design upgrades version 1.4 optimizing the design

On a side note, I have registered my package design Patent used on the 1st page in Canada. In regards to the new BIOS chip design, I believe that I have developed a new method or process for BIOS based encryption the equations have been tested four times and should be valid. Chapter 5 presents a short presentation of the Hard Disk and Memory chips configuration coupled with Menu Screen encryption process developed in chapter 4 using 88128 bits using 648 * 136 cycles.

This Rom chip design has been completed and optimized for middle grade servers. This Rom Chip version includes using the new BIOS Encryption process that has been designed. The menu screen contains is designed for the 648 pin bios chip design ver 1.5 .

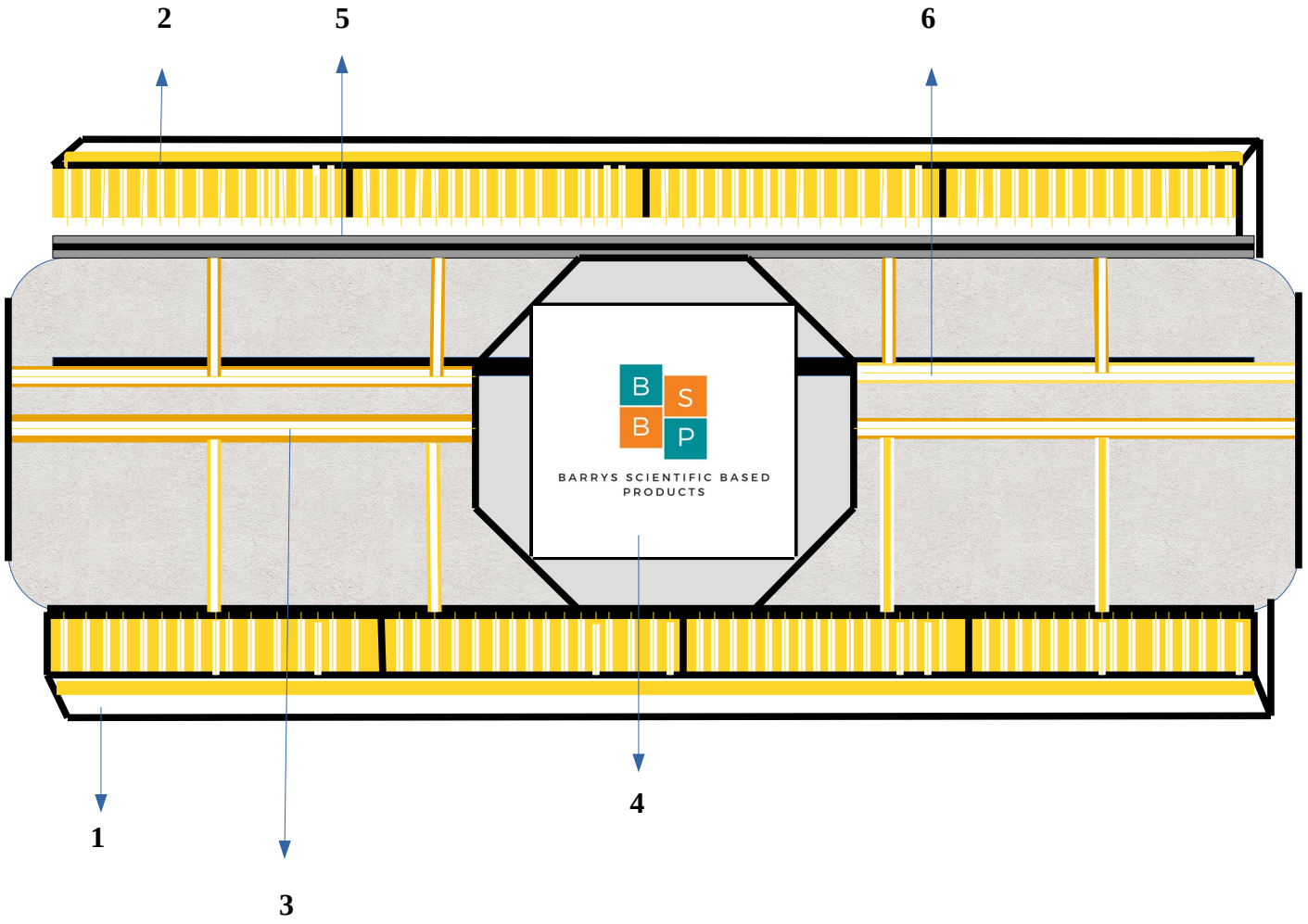
This design represents the last upgrade for this platform of Bios and Chip designs. This design optimizes version 1.4 which would be considered minor revisions but they are needed to make the best of this Chip design via optimization.

Table of Contents

Visual Design

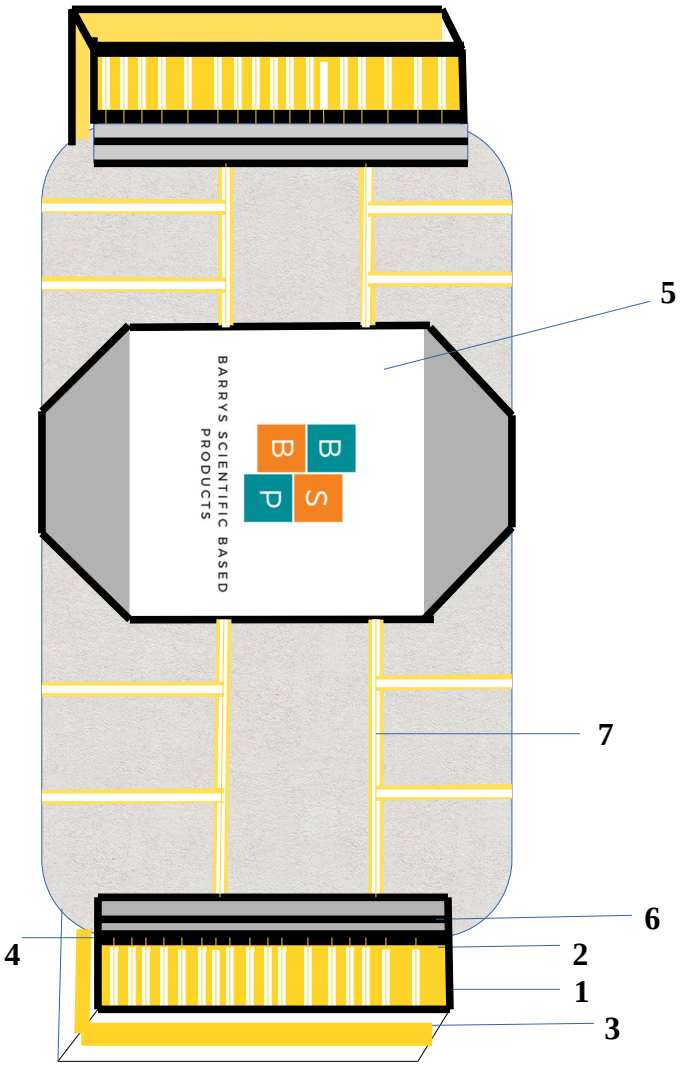
Chapter 1

Bios Chip Design ver 1.5/648 Chart 1-A



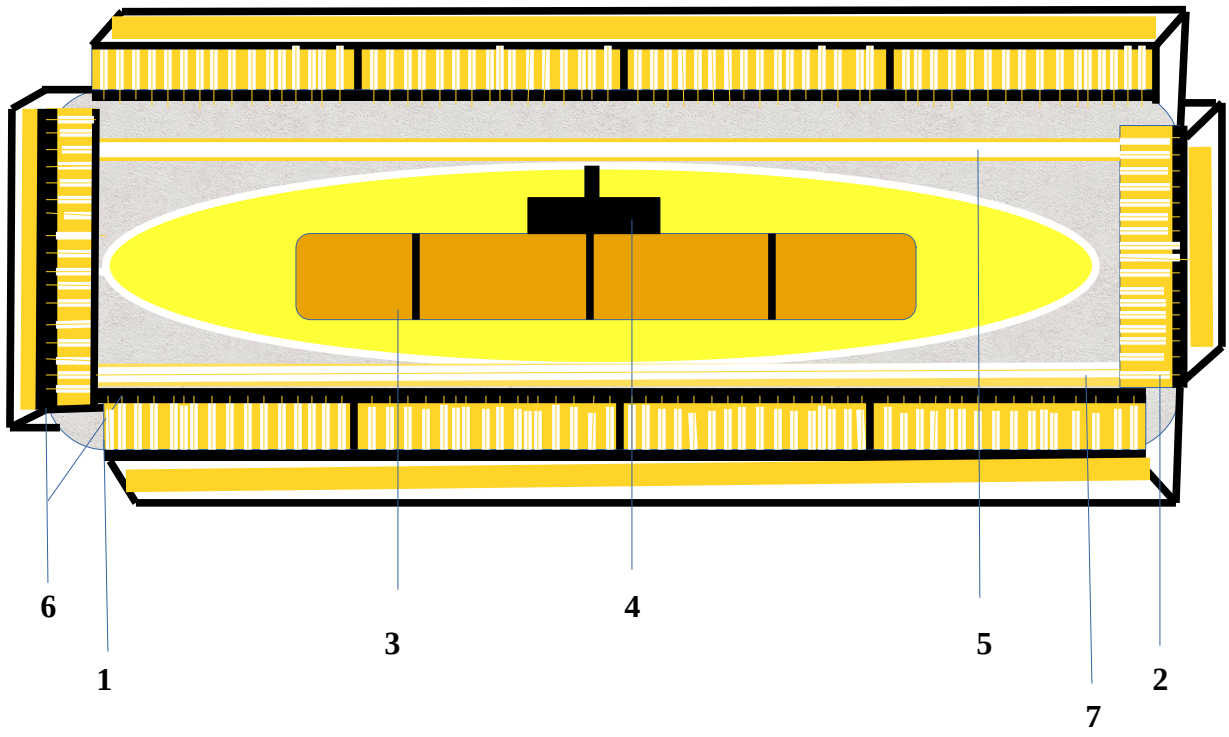
1). Dual sided Pins 64 * 2 = 128 Slot 1 and 2 total 256 .10 cm titanium plated Copper inside
2). Dual sided Pins 64 * 2 = 128 Slot 3 and 4 total 256 .10 cm titanium plated Copper inside
3). Titanium Plated with thin fiber optic wiring inside.
4). Logo placed on Bios chip
5). Internal Bridge Pins to Fiber Optic wiring
6). Thin wire used for tunnelling protocols

Bios Chip Design rev 1.5/648 Horizontal Pins Chart 2-A



1). 34 pins per side total 136 pins (scaled on chart 2-a 16 pins on Design)
2). Pins .10 Titanium plated copper inside
3). Dual sided bank 17 pins * 2 =34 pins
4). Heat shield
5). Logo placed on chip
6) Bridge to network paths
7). Thin wire used for tunnelling protocols

Bios Chip Design ver 1.5/648 Chart 3-A Back view



1). Dual sided Pins 64 * 2 = 128 Slot 1 and 2 total 256 .10 cm titanium plated Copper inside
2). Dual sided Pins 17* 2 =34 slot 1 and 2 = 136 .10 Titanium copper plated inside
3). Buffer 4 spaces 34 per cycle total 136 cycles
4). Bridge
5). Data path from and to Pins
6). Heat shields
7). Thin wire used for tunneling protocols

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 648 pins 128*4 and 34*4 that is dual sided. In chart 1-a I configured the pins and are represented by showing the front side of the pins that are dual sided. The side of the chip has a dual side as well. The pin composite is .10 cm Titanium plated outside and copper inside. The design deploys heat shields as well The front side has 4 wires for a total of 8. Wires on the side are not split. This Bios chip is capable of running the CPU I previously designed 648 bits. This allows encryption to take place masking the BIOS and CPU's and now hard disk raided with memory. The encryption ring uses .20 cm making thicker wires to push more bits through.

The BIOS chip also has Thick wires that are copper plated .20 cm titanium inside copper .10 cm along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches. I have added thin wires for the purpose of loading tunnelling protocols inside the wiring.

On the back side of the BIOS chip see chart 3-A has a thick fiber optic ring network topology and four buffers with a way to pipe more bits to the mother board and uses I/O Scheduling allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption process and or method

Encryption method for Password

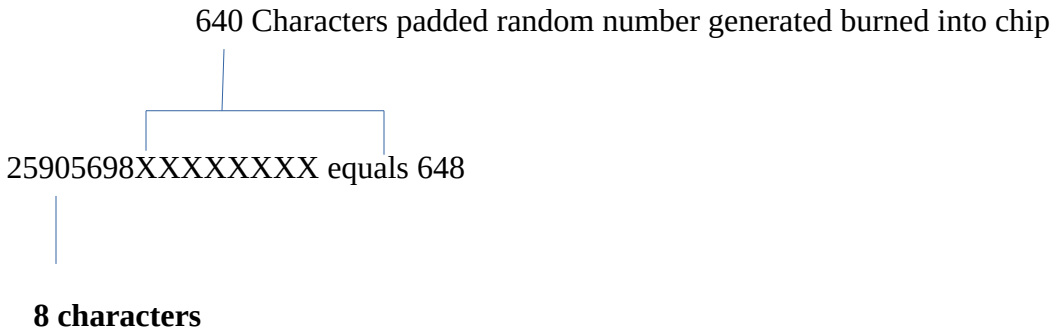
BIOS Pins	# Cycles	CPU used	padded bits
648	8	648	4536
648	16	648	9720
648	24	648	14904

Equation Equals BIOS Pins * Number of cycles minus CPU

BIOS Pins	#CPU	Password field length	Bit Strength
648	648	38	5184
648	648	76	10368
648	648	114	15552

Equation is CPU add padded bits/136 equals password length = Bit Strength

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 4536 Padded Bits plus 648 / 648 equal 8 characters for my security key because I am allowed 648 characters I can than pad the other 640 characters for my security key thus my security key would look like this below:



If I took 9720 plus 648 / 648 I could use 16 characters and 648 minus 16 I can use 632 characters for padding also 14904 padded plus 648 /648 equals 24 Characters with 624 character padding. **This is a example of only 1 cycle if you turn to the next page I use 8 cycles for my process.**

Real Characters	**Padded Characters**	**Constant 136**
8	640	648
16	632	648
24	624	648

Security Key Encryption

CPU	Constant = 648 bits	#Characters	Character pad
648	**648**	**8**	**640**
648	**648**	**16**	**632**
648	**648**	**24**	**624**

Equation = 1). CPU*8 /648 = #Characters

A = 648

2). A – Character Representation = Character Padding

This idea would create 3 security keys used for the CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key 648 equals Password Length 648

Each security key is different and unique depending on the encoding scheme used. The Equation takes a CPU multiply by eights divide by 648. The 2nd step is declare A =648. The 3rd step is A – Character representation gives you the amount of padding you can use which represents character representation. because I am allowed a total of 648 characters using the method and adding the padding I can now extend my security keys to 648 characters.

Chapter 4

Menu Screen

Date mm/dd/yyyy/ade **88128 Bits Menu Screen**

Time 000:000:000

Barrys Scientific Based Products BIOS Software

Bios Chip ver 1.5

1). CPU 648 Bits

2). Password Security

3). Raided Disk

4). Hard Disk Encryption “y or n”

5). BIOS Menu Encryption

6). Memory Encryption “y or n”

7). USB Device Encryption

8). Mouse Encryption

9). Communications

10). Keyboard Encryption

11). Tunneling Wire enable “y or n”

Bios Menu Screen Updates ver 1.5

The following updates have been applied for this Bios Menu Screen

1). Screen is encrypted using 88128 Bits @ 648 * 136

2). Enabling tunnelling protocol

3). The time Field has been added with microseconds included This also will protect against server certificates and misconfigurations do to misuse of time fields.

Chapter 5

Hard Disk and Memory Encryption

After reviewing Chart 3-a, I can now create Hard Disk and Menu Screen Encryption because I have a BIOS chip that has a builtin Network Topology Hardware and System level software based on the following parameters:

1). Bios Pins 136 cycles
2). assigned variable 88128 Bits

The Equation is 88128 bits / 136 cycles = 648 based on the hardware using thick wires it would take 136 cycles to encrypt the hard disk whether raided or not and now Memory Chips. This would create bottle necks. The solution is to create four area buffers to load the cycles into the Data Pipe meaning each buffer could load 34 cycles since there are four and would equal 136 cycles. This would alleviate bottle necks by using the I/O scheduling mechanisms for each buffer space.

Chapter 6

Final Thoughts

This Bios chip and was designed for Middle range servers using a 648 bit CPU.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it's number of bits maximum 88128 bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is now using a newly designed mathematical process and or method working with 136 cycles instead of 128. In previous works, I used the newly designed process and it is now valid because it has been shown to work on four different occasions with this design not using a sequential pattern. I have updated the Menu Screen using this BIOS chip at 88128 bits encrypted. The menu screen has been updated to enable tunnelling protocols.

The BIOS chip uses 648 pins with the backside of the chip using a thicker internal fiber optic ring topology that utilizes encryption to protect the BIOS software. I have created four buffer areas that would allow for hard disk, memory, USB encryption, keyboard, mouse using 88128 bits. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a CPU that has access to three different security keys based on previous CPU design I have written. I have begun to place a manufacturer label on my Rom Chip please see chart 1 and 2-a.

This is the last version of this new chip design it has been fully optimized and upgraded to 88128 bits > 65536 standard PC's also instead of 128 cycles this design is capable of going to 136 cycles and is configured to do so.

I would like to thank each and everyone of you for viewing this work

If you wish to see further work please go to the following website below:

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05/13/2023