

Barry's 648 Bit CPU and 729 Wiring Block Configuration

By

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Introduction

I have created a new CPU Design that accesses directly a ring Network Typology creating 12 areas of space on the overall ring 8 external spaces and 4 Internal spaces coupled with 12 node points to create linear paths and circular motion for a new encryption method and or technique.

My design will be geared toward the title “Barry's 648 bit CPU and 729 Wiring Block Configuration” . I am using a single network Topology Design configured for 12 areas of space with 12 node points on the Network Ring for encryption.

I have updated the wiring configuration now using 9 bit processing instead of the standard 8 bits to build a new CPU architecture. 9 wires at 81 bits for a total of 729. The wiring block configuration will be different than the CPU and will require a algorithm using a clip board for cycle processing . The Asymmetry in this is the CPU Processes 648 Bits 6 wires at 108 bits and the Ring Network Topology utilizes 729 bits 9 wires at 81 bits.

The Algorithm has been setup using the number 9 and cycle processing to use Linear paths via Node Points than it goes to the Concentric Circle and goes around it depending on the BIOS software wiring configuration thus I have established both Linear and Circular Motion.

The main idea of this work is building 9 Bit Processing Architecture.

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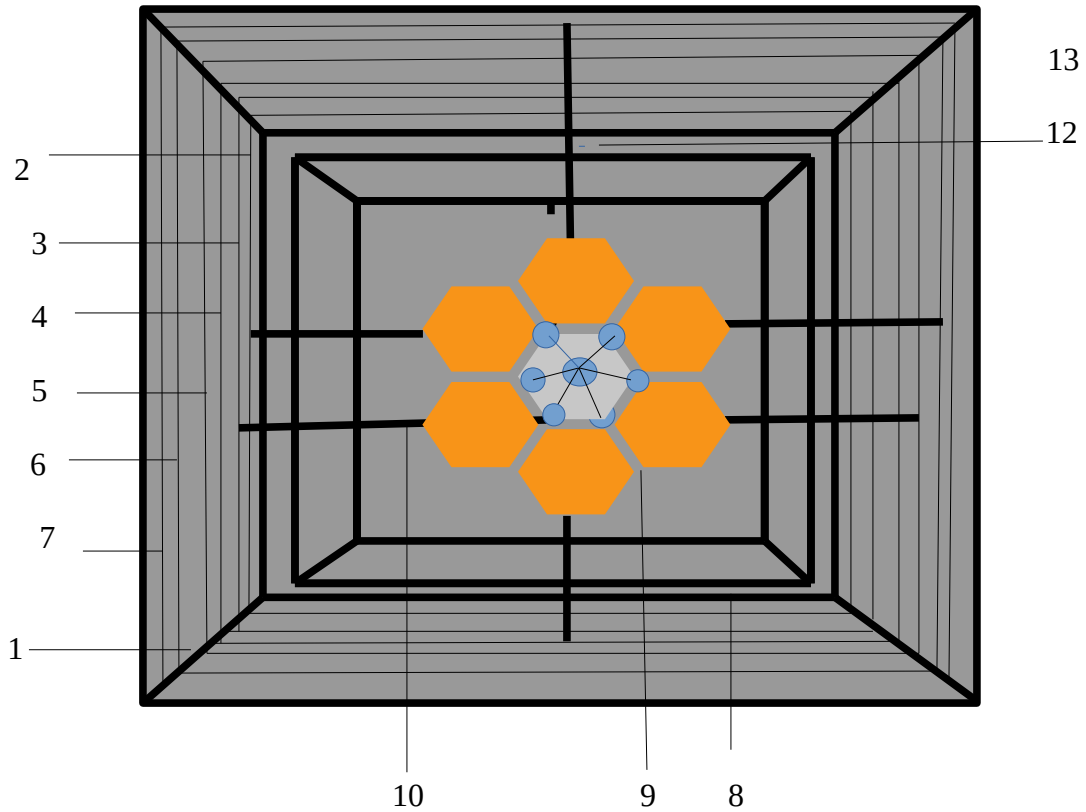
- 1). Chapter 1 Visual Design
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- 3). Chapter 3 Data Table
- 4). Chapter 4 Menu Screen for 729 Bit CPU
- 5). Chapter 5 Final Thoughts

Chapter 1

Visual Design

648 BIT CPU Visual Chart 1-A

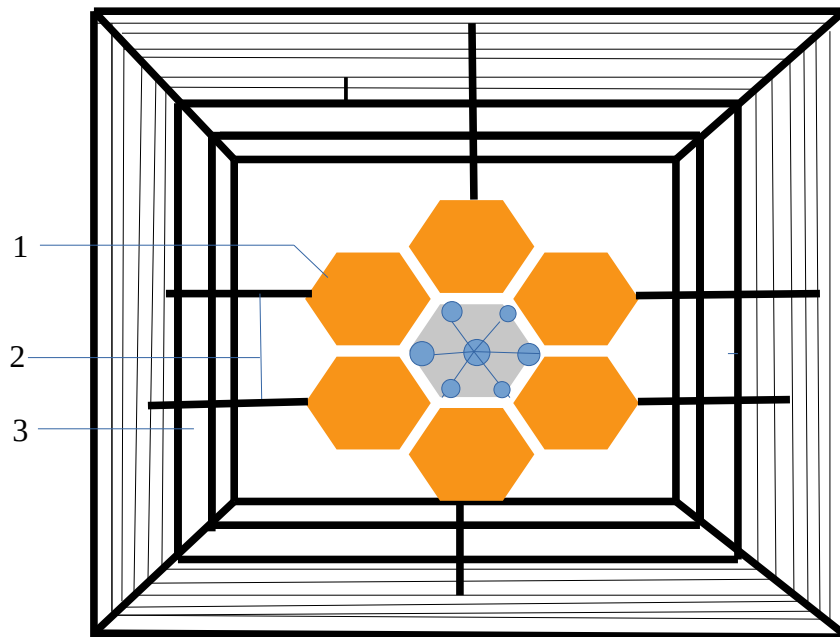
General View



- 1). Case Holder
- 2). Wire 1 108 Bits
- 3). Wire 2 108 Bits
- 4). Wire 3 108 Bits
- 5). Wire 4 108 Bits
- 6). Wire 5 108 Bits
- 7). Wire 6 108 Bits
- 8). case fitting for CPU's
- 9). CPU 1 (648) Bits 6 External spaces, 1 Internal Topology shell, 6 Gateways
- 10). 1-6 wires connected with 6 gateways

648 BIT CPU Visual Chart 2-A

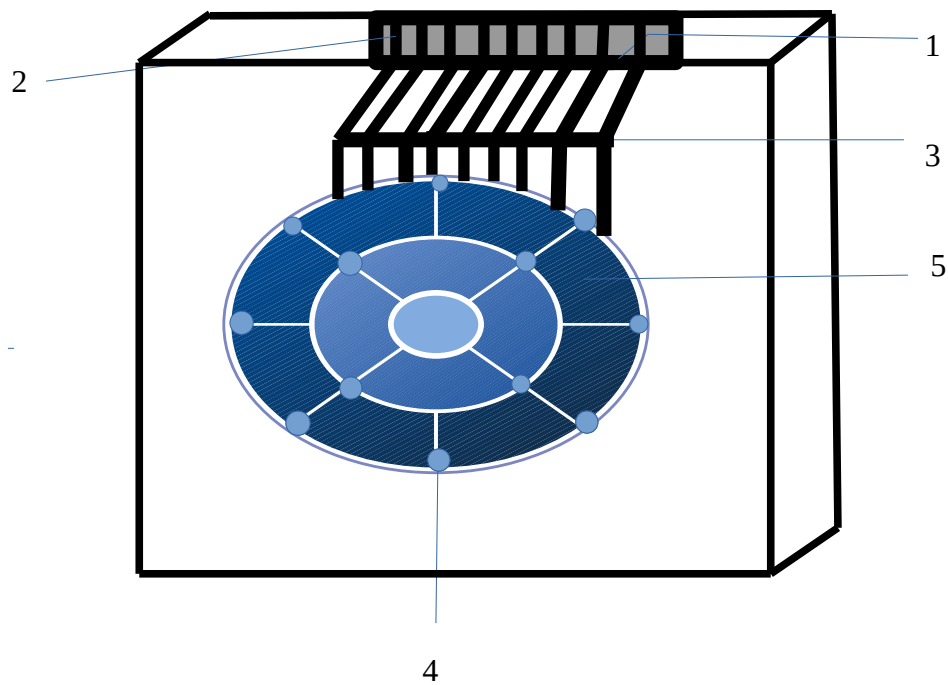
Inside Front View



- 1). CPU 1 (648) Bits 6 External spaces, 1 Internal Topology shell, 6 Gateways
- 2). Wires 1- 6 108 bits per wire
- 3). Case Fitting

729 BIT CPU Do decagon Visual Chart 3-A

Wiring Block and Inside Ring Network



- 1). Terminator Block
- 2). 9 wires thick .20 cm = 81 bits per wire total 729 bits
- 3). Terminator Block
- 4). 12 Node Points
- 5). Ring Network Topology

Chapter 2

Specifications

I will now go over the specifications. The Shape of the CPU Design uses a octagon 6 sided Polygon to create 6 External spaces with 6 Internal Gateways for a total of 648 Bits 6 wires at 108 bits.

The wiring block for the Network Ring with thick wires uses the following .20 cm = 81 bits for a total of 729 bits. As stated earlier, The CPU has 6 wires at 108 bits. The wiring block uses 9 wires at 81 bits for a total of 729 Bits.

The CPU has a built in Network Typology's to create 12 areas of space also created on the rings are Node Points that uses linear paths and accesses a concentric circle built on the CPU that has access to it. The concentric circle and linear paths can now create encryption shielding CPU's from BIOS based attacks instead of broadcasting Bios based software. The total node points are 8 external and 4 internal for a total of 12. The point within the Internal Shell allows it to access the built in Network Topology this demonstrates the principle of Dimensional space from the CPU to the Network Topology no point of origin if you notice only acting as a gateway.

The Ring Network is configured for the CPU . The back of the CPU has Bridge two terminator blocks on the bridge. Please also note the Network Topology utilizes linear and circular motion in processing data to the CPU's.

After the bridge, The final switch that goes to the wires processes 729 bits per cycle on the Network Ring to create encryption for the CPU's. This creates the following concepts:

- 1). 9 Bit Processing.
- 2). CPU 648 bits and Wiring Block 729 bits are Asymmetrical.
- 3). Bit processing on the Wiring Block are now capable of using a clipboard that can utilize cycles thereby protecting the CPU Instruction sets.

I have created five different wiring configurations used for the BIOS. This particular design does not accept anything less than 729 bits. This avoids cloning a CPU and it's software because of the Unique Configuration, wiring, and design.

Switch/Terminal Block Configuration Chart 4-A

X1 = CPU1on
Z = Off

X1 Wires On and number of cycles

wire 1 CPU 1	81 bits	X1	{1,2,3,4,5,6,7,8,9 }
wire 2 CPU 1	81 bits	X1	
wire 3 CPU 1	81 bits	X1	
wire 4 CPU 1	81 bits	X1	
wire 5 CPU 1	81 bits	X1	
wire 6 CPU 1	81 bits	X1	
wire 7 CPU 1	81 bits	X1	
wire 8 CPU 1	81 bits	X1	
wire 9 CPU 1	81 bits	X1	
CPU 1 Total Bits		729 Bits	

X3 Wires On and number of cycles

wire 1 CPU 1	81 bits	X3	{1,2,3,4,5,6,7,8,9 }
wire 2 CPU 1	81 bits	X3	
wire 3 CPU 1	81 bits	X3	
wire 4 CPU 1	81 bits	X3	
wire 5 CPU 1	81 bits	X3	
wire 6 CPU 1	81 bits	X3	
wire 7 CPU 1	81 bits	X3	
wire 8 CPU 1	81 bits	X3	
wire 9 CPU 1	81 bits	X3	
CPU 1 Total Bits		729 Bits * 3 cycles = 2187	

X9 Wires On and number of cycles

wire 1 CPU 1	81 bits	X9	{1,2,3,4,5,6,7,8,9 }
wire 2 CPU 1	81 bits	X9	
wire 3 CPU 1	81 bits	X9	
wire 4 CPU 1	81 bits	X9	
wire 5 CPU 1	81 bits	X9	
wire 6 CPU 1	81 bits	X9	
wire 7 CPU 1	81 bits	X9	
wire 8 CPU 1	81 bits	X9	
wire 9 CPU 1	81 bits	X9	
CPU 1 Total Bits		729 Bits * 9 cycles = 6561	

X27 Wires On and number of cycles

wire 1 CPU 1	81 bits	X27	{1,2,3,4,5,6,7,8,9 }
wire 2 CPU 1	81 bits	X27	
wire 3 CPU 1	81 bits	X27	
wire 4 CPU 1	81 bits	X27	
wire 5 CPU 1	81 bits	X27	
wire 6 CPU 1	81 bits	X27	
wire 7 CPU 1	81 bits	X27	
wire 8 CPU 1	81 bits	X27	
wire 9 CPU 1	81 bits	X27	
CPU 1 Total Bits		729 Bits * 27 cycles = 19683	

Chapter 3

Data table

Table

Please note the total number of bits are divided by 9 making it qualified as a 9 bit processing system. If we compare 8 bit processing verse 9 bit processing, We find that 9 bits with cycles greatly exceeds the 8 bit processing see below:

$$8 * 1 = 8 \quad 1^{\text{st}} \text{ power}$$

$$9 * 1 = 9 \quad 1^{\text{st}} \text{ power}$$

$$8 * 8 = 64 \quad 2^{\text{nd}} \text{ power}$$

$$9 * 9 = 81 \quad 2^{\text{nd}} \text{ power}$$

$$8 * 8 * 8 = 512 \quad 3^{\text{rd}} \text{ power}$$

$$9 * 9 * 9 = 729 \quad 3^{\text{rd}} \text{ power}$$

$$8 * 8 * 8 * 8 = 4096 \quad 4^{\text{th}} \text{ power}$$

$$9 * 9 * 9 * 9 = 6561 \quad 4^{\text{th}} \text{ power}$$

$$8 * 8 * 8 * 8 * 8 = 32768 \quad 5^{\text{th}} \text{ power}$$

$$9 * 9 * 9 * 9 * 9 = 59049 \quad 5^{\text{th}} \text{ power}$$

9 Bit Processing

1 st	729 /9	= 81
2 nd	2187/9	= 243
3 rd	6561/9	= 729
4 th	19683/9	= 2187
5 th	59049/9	= 6561

The number used for total bits after cycles are divisible by 9 showing that it is a workable solution.

On another note, The CPU uses 648 bits at 6 wires 108 bits per wire while the Wiring block uses 729 bits at 9 wires for 81 bits. These configurations are easily divisible by 9 see below

$$\text{CPU} \quad 648 / 9 = 72$$

$$\text{Wiring Block} \quad 729 / 9 = 81$$

If we subtract 81 -72 we have a number of 9 used for the processing and architecture for this design. What this shows is the CPU with its 648 bits goes to the Bridge of the Network Ring Topology and is expanded allowing for 9 bit encryption algorithms to process within the Network Topology. The Ring Network Topology cannot go back to the CPU to process information thus it protects the CPU from being cloned and registers are protected because of this feature.

I will now proceed to the next chapter creating menu screens to be used in BIOS software.

Chapter 4

Menu Screen for 729 Bit Wiring Block

I would like to make a few notes and they are the following:

- 1). The CPU processes 648 bits whereas the Ring Network processes 729 bits.
- 2). The Wire usages 1 – 9 use 1 thick .20 cm with 9 wires at 81 bits for a total for 729 bits.
- 3). The encryption takes the wiring block configuration along with the BIOS software using 9 bit processing with the ring Network using cycles this is illustrated in the Data tables.

729 Wiring Block Configuration

- 1). CPU 1 and Ring Network 1 “Enable yes or no”
- 2). Wire x1 729 bits “Enable yes or no”
- 3). Wire x3 2187 bits “Enable yes or no”
- 4). Wire x9 6561 bits “Enable yes or no”
- 5). Wire x27 19683 Bits “Enable yes or no”
- 6). Wire x81 59049 Bits “Enable yes or no”

Rem X number = number of cycles

Rem BIOS Software does not accept anything less than 729

I will now finish this work with my final thoughts in the next chapter.

Final Thoughts

Chapter 5

1). I have completed a new 648 Bit Octagon CPU Design with 729 wiring block configuration. This design uses a Octagon Shape CPU coupled with ring Network Topology along with 9 bit architecture processed for CPU , Ring Network Topology, and Encryption.

2). The wiring block has five different configurations used in the BIOS also creating a new Algorithm in comparison to the standard 8 bit CPU architecture the tables in Chapter 3 provide the Information.

3). I have installed terminator blocks on the switches to control the Input and Output of the switches 0 = off 1 = on.

4). The 648 bit CPU directly accesses the 729 Bit ring Network Topology that uses Linear and Curvature motion also creating Encryption.

5). I have added in this design a switch/terminal block configuration see chart 4-a with 5 different wiring configurations that can be custom configured in the BIOS screen.

6). This Design deploys 9 bit architecture.

7). **The Barry Infinity Equality Field equation** has been represented as a practical application by using a Gateway on the CPU that accesses the Ring Network Topology creating two different objects and used as a dimension space portal application as a means of demonstrating unification of two different objects through the number 9.

8). I have now built on my CPU's a Internal Network Topology Design that will be used for future Motherboard Designs.

I would like thank each and everyone of you for viewing this work because it is worth considering. To view more works please go to the website below.

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