

 *Barrys Scientific Based Products*





Barrys Scientific Based Products BIOS Chip ver 1.1

By

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Introduction

I would like to thank you for taking the time in viewing this work. I have designed and upgraded a BIOS chip that interfaces with the CPU's I have previously designed specifically 128, 256, 384. These CPU's are designed for low end to Middle range servers small to medium level businesses. The new chip Design offers integration with better security approaches taken. The BIOS chip is a 48 pin wire chip with a built in Ring topology that offers encryption to protect system level based software. The chip has built inside 3 objects that are used for the CPU's as mentioned above. This system is geared more to Linux and Unix based systems.

On a side note, I am introducing my new packaging design on the 1st page. In regards to the new BIOS chip design, I believe that I have developed a new method or process for BIOS based encryption.

The Rom chip will continue to go through future updates or revisions. This Rom Chip version presents a more developed BIOS Encryption mechanism. Future developments will be needed on this chip design.

I have begun to develop a menu screen for the BIOS software that will be included in future updates.

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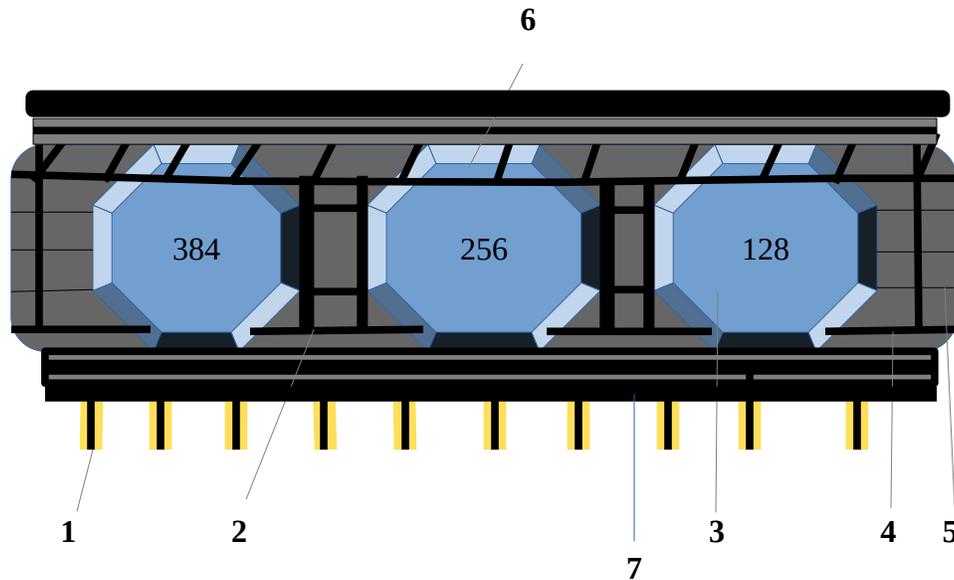
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Visual Design

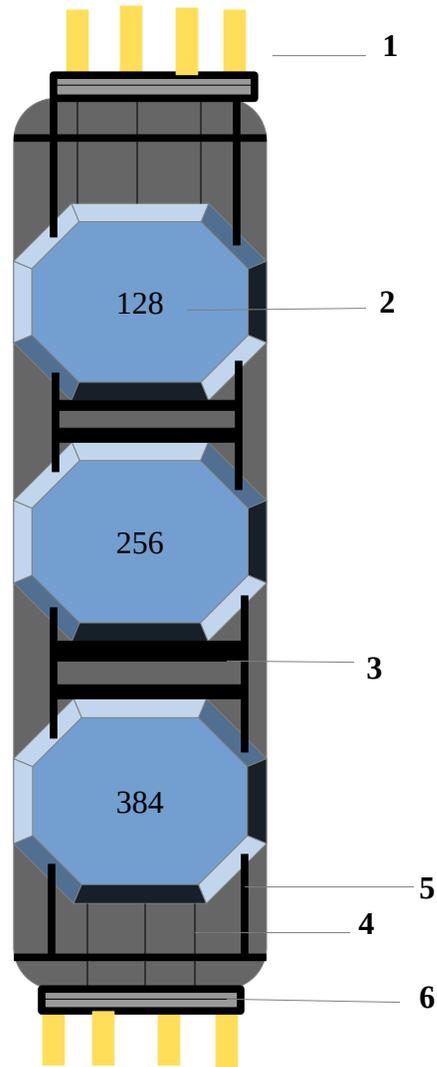
Chapter 1

Visual Chart 1- A BIOS Chip General View



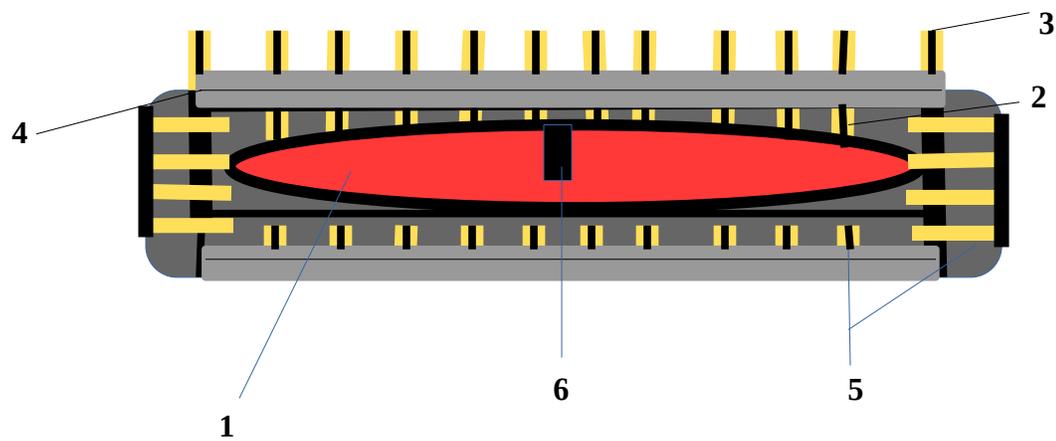
- 1). Pins to chip 20 on Each side total 40 pins .30 cm split pin copper .15 per split
- 2). Switches to 3 CPU's 384, 256, 128 4 total Internal
- 3). 3 CPU's 384, 256, 128
- 4). Thick wire .10 cm
- 5). Thin wire
- 6). Wire to Pins .10 cm
- 7). Heat shield

Visual Chart 2- A BIOS Chip Front View



- 1). **Front side Pins 4 on each Side total 8 Pins copper .30 cm**
- 2). **3 CPU's 128, 256, 384**
- 3). **Switches to CPU's total 4 Internal**
- 4). **Thin wire**
- 5). **Thick wire .10 cm**
- 6). **wire to Pins**

Visual Chart 3- A BIOS Chip Back View



- 1). Thick Fiber Optic Ring .20 cm Encryption
- 2). Back side of Pin touches Thin Fiber Optic
- 3). Front Side of Pin
- 4). Thin wiring
- 5). Total Pins 48
- 6). Data piped to motherboard

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 48 wires 20 on each side each split and 1 actually equals 2 pins for a total of 40. The pin thickness is .30 with each pin .15 cm. The front side has 4 wires for a total of 8. Wires on the side are not split. The Bios chip is capable of running the CPU's I previously designed 128, 256, and 384 bits. This allows encryption to take place masking the BIOS and CPU's. The encryption ring uses .20 cm making a thicker wire to push more bits through the wire

The BIOS chip has Thick wires .10 cm and thin wires along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches.

On the back side of the BIOS chip see chart 3-A has a thin fiber optic ring network topology with a way to pipe more bits to the mother board allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption process and or method

Encryption method for Password

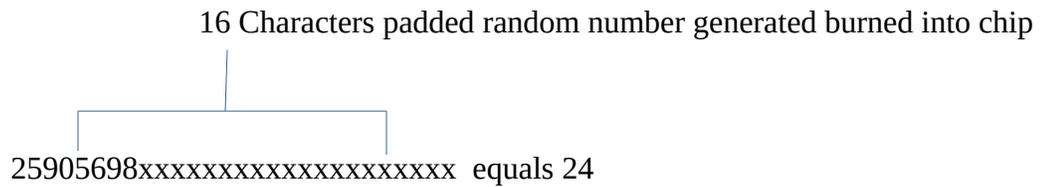
BIOS Pins	# Cycles	CPU used	padded bits
48	8	128	256
48	16	256	512
48	24	384	768

Equation Equals BIOS Pins * Number of cycles minus CPU Used

BIOS Pins	#CPU	Password field length	Bit Strength
48	128	24	3072
48	256	32	8192
48	384	32	12288

The Equation is Bit strength / CPU equals password length add padded bits

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 128 Padded Bits $256 / 48$ equal 8 characters for my security key because I am allowed 24 characters I can than pad the other 16 characters for my security key thus my security key would look like this below:



If I took 256 plus $512 / 48$ I could use 16 characters and 16 characters padding also 384 plus $768 / 48$ equals 24 Characters with 8 character padding. Please see chart on next page.

Security Key Encryption

CPU	Constant = 48 bits	#Characters	Character pad
128	48	8	16
256	48	16	16
384	48	24	8

Equation = CPU Plus Padded Bits /48 = Character representation – password field length.

This idea would create 3 security keys used for each CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key equals Password Length

Each security key is different and unique depending on the CPU used. The Equation takes a CPU multiply's the number of cycles and divides it by 48 which represents character representation because I am allowed 24 or 32 characters dependent on field length I subtract the actual characters minus password length and allows for additional padding. I will now present my final thoughts in the next chapter.

Chapter 4

Menu Screen

Barrys Scientific Based Products BIOS Software

- 1). CPU 128 Bits
- 2). CPU 256 Bits
- 3). CPU 384 Bits
- 4). Password Security

Chapter 5

Final Thoughts

The Bios chip is designed for low end to Middle range servers using 128, 256, and 384 Bit CPU's previously designed for small and middle range businesses.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it's number of bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is now using a mathematical process and or method working with 48 bits. I have begun to develop a Menu Screen using this BIOS chip

The BIOS chip uses 48 pins with the backside of the chip using a thicker internal fiber optic ring topology that utilizes encryption to protect the BIOS software. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a selection of 3 different CPU's as a selection based on previous CPU designs I have written.

I would like to thank each and everyone of you for viewing this work !

If you wish to see further work please go to the following website below:

www.barryscientificbasedproducts.com

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