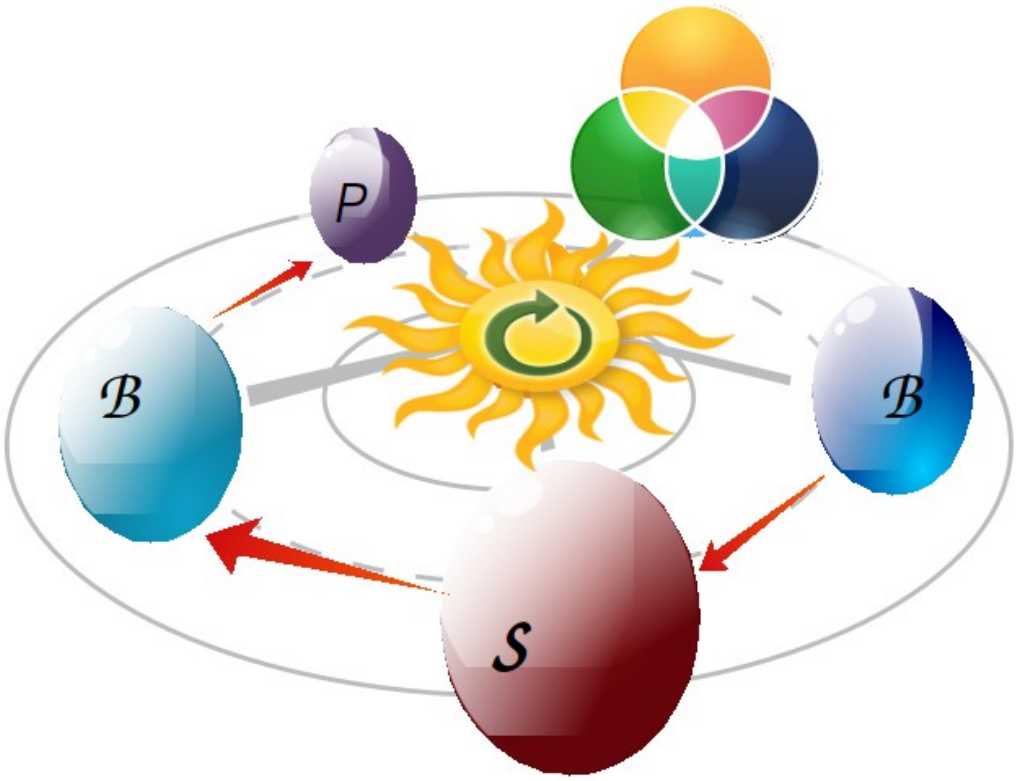


Barrys Scientific Based Products

Barrys Scientific Based Products BIOS Chip ver 1.3

By

Barry L. Crouse

Introduction

I would like to thank you for taking the time in viewing this work. I have designed and upgraded a BIOS chip that interfaces with the CPU's I have previously designed specifically 128, 256, 384. These CPU's are designed for low end to Middle range servers small to medium level businesses. The new chip Design offers integration with better security approaches taken. The BIOS chip is a 128 pin wire chip titanium plated with the inside using copper wires and built in Ring topology that offers encryption to protect system level based software. The new Bios chip comes with two buffers to process 16384 bits at 128 cycles.. This system is geared more to Linux and Unix based systems.

On a side note, I am introducing my new packaging design on the 1st page. In regards to the new BIOS chip design, I believe that I have developed a new method or process for BIOS based encryption the equations have been tested twice and should be valid. Chapter 5 presents a short presentation of the Hard Disk and Memory chips along with Menu Screen encryption process developed in chapter 4 using 16384 bits.

This Rom chip design has been completed for low to middle grade servers. This Rom Chip version includes using the new BIOS Encryption process that has been designed. I have begun to utilize hard disk and memory encryption on the Chip see chapter on visual design and chapter 5. The menu screen contains a basic outline for this design and will be further developed when I start working on high grade servers in the future.

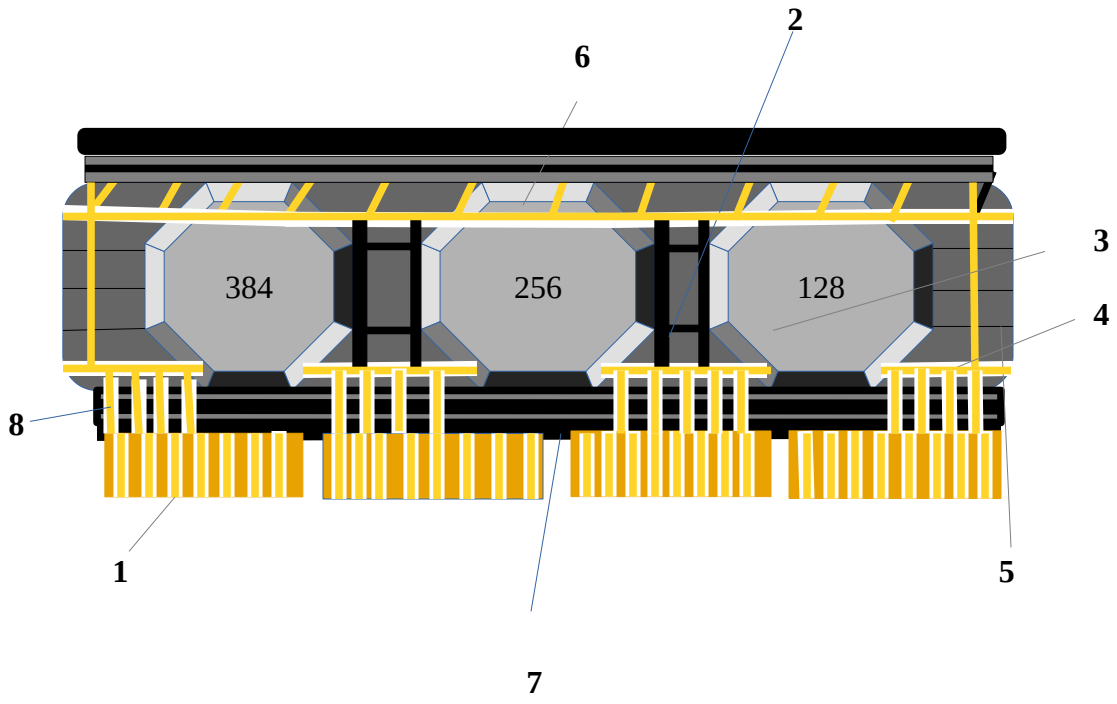
I have updated the menu screen for the BIOS software and will be updated further in higher grade servers also I put in the menu screen USB Device Encryption is now to protected against ports that are vulnerable to Cyber attacks also because I have encountered date misconfigurations on my own server I have added a date Field that is also encrypted in nature with a explanation on the extension of the Date Field.

Table of Contents

Visual Design

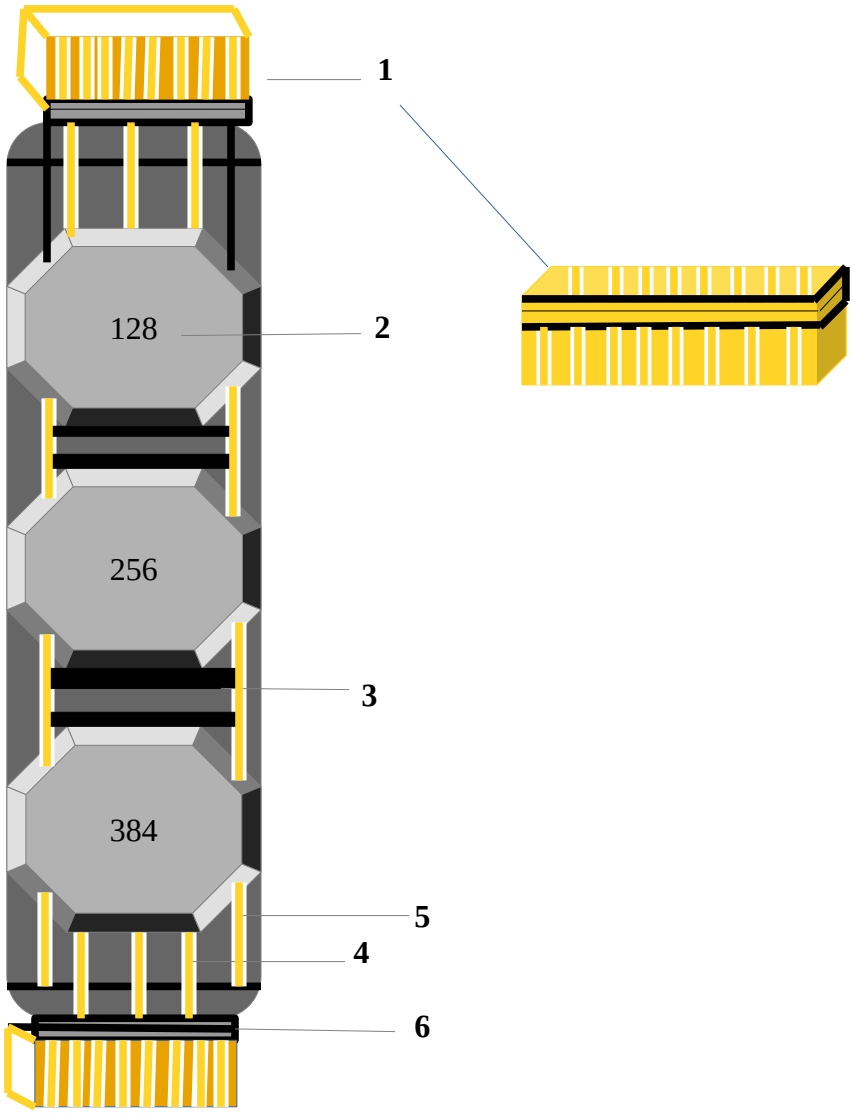
Chapter 1

Visual Chart 1- A BIOS Chip General View



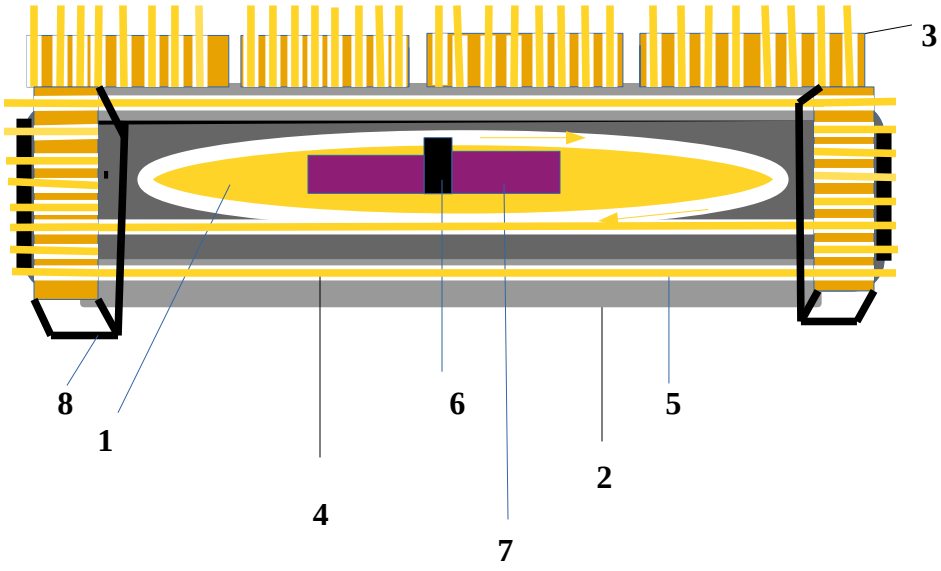
1). Bank 1 4 banks each bank 8 pins 32on each side .20 cm white = titanium .10 light gold = copper
2). Switches to 3 CPU's 384, 256, 128 4 total Internal
3). 3 CPU's 384, 256, 128
4). Thick wire .20 Titanium plated .10 copper
5). Thin wire
6). Wire to Pins .10 cm
7). Heat shield
8). Bank 2 4 banks each bank 4 pins 16 on each side .20 cm white = titanium .10 light gold = copper

Visual Chart 2- A BIOS Chip Front View



1). Dual side Pins 16 on each Side total 32 Pins Titanium white plated .20 cm light gold copper .10 cm Bank 1 8 Pins Bank 2 8 Pins
2). 3 CPU's 128, 256, 384
3). Switches to CPU's total 4 Internal
4). Thick wire Titanium white plated .20 cm light gold copper .10 cm
5). Thick wire .20 cm titanium plated .10 cm copper
6). wire to Pins

Visual Chart 3- A BIOS Chip front Back View



1). Thick Tiber Optic Ring .20 cm Encryption
2). Back side of Pin touches Thin Fiber Optic
3). Pin Composite White Titanium Plated .20 cm light gold copper .10cm
4). Composite White Titanium Plated .20 cm light gold copper .10cm
5). Total Pins 128 Vertical 96 pins horizontal 32
6). Data piped to motherboard
7). two buffer area linked to data pipe
8). Dual sided pins each side 16 total 32pins

Chapter 2

Specifications

I will now go over the specifications or specs for this Bios Chip. The chip has 128 pins 48*2 and 16*2 for each side. In chart 1-a I configured the pins are represented in Banks stacking one on top of another. The side of the chip has a dual side overlaying next to one another. The pin composite is .20 cm Titanium plated and .10 cm copper. The front side has 4 wires for a total of 8. Wires on the side are not split. The Bios chip is capable of running the CPU's I previously designed 128, 256, and 384 bits. This allows encryption to take place masking the BIOS and CPU's and now hard disk raided with memory. The encryption ring uses .20 cm making thicker wires to push more bits through.

The BIOS chip also has Thick wires that are copper plated .20 cm titanium inside copper .10 cm along with this comes Internal switches 4 in total that checks the CPU to load into the BIOS hint off and on switches.

On the back side of the BIOS chip see chart 3-A has a thick fiber optic ring network topology and two buffers with a way to pipe more bits to the mother board and uses I/O Scheduling allowing for encryption to take place when making configurations inside the BIOS. The energy in motion uses both circular when using cycles and linear for piping data to the Board. The Encryption technique or method is in the next chapter;

Chapter 3

BIOS Chip Encryption process and or method

Encryption method for Password

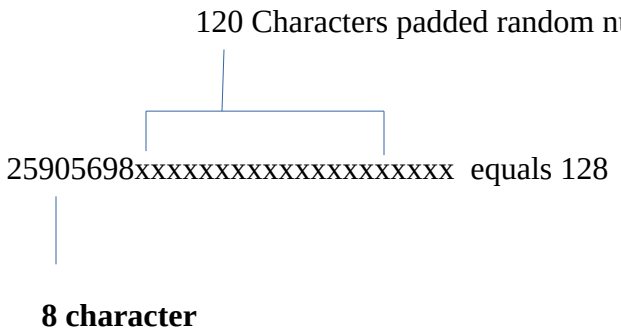
BIOS Pins	# Cycles	CPU used	padded bits
128	8	128	896
128	16	256	1792
128	24	384	2688

Equation Equals BIOS Pins * Number of cycles minus CPU

BIOS Pins	#CPU	Password field length	Bit Strength
128	128	8	1024
128	256	16	2048
128	384	24	2688

Equation is CPU add padded bits/128 equals password length = Bit Strength

As you can see, The password length has been extended but this does not guarantee absolute security. One additional method would be to add a security key static to match the password length but in a asymmetric manner. I will take 896 Padded Bits plus 128 / 128 equal 8 characters for my security key because I am allowed 128 characters I can than pad the other 120 characters for my security key thus my security key would look like this below:



If I took 1792 plus 256 / 128 I could use 16 characters and 128 minus 16 I can use 112 characters padding also 2688 padded plus 384 /128 equals 24 Characters with 104 character padding. **This is a example of only 1 cycle if you turn to the next page I use 8 cycles for my process.**

Real Characters	**Padded Characters**	**Constant 128**
8	120	128
16	112	128
24	104	128

Security Key Encryption

CPU	Constant = 128 bits	#Characters	Character pad
128	**128**	**8**	**120**
256	**128**	**16**	**112**
384	**128**	**24**	**104**

Equation = 1). CPU*8 /128 = #Characters

A = 128

2). A – Character Representation = Character Padding

This idea would create 3 security keys used for each CPU thus by using Asymmetrical principles of energy I have created equality by the following statement below:

Security Key 128 equals Password Length 128

Each security key is different and unique depending on the CPU used. The Equation takes a CPU multi ply by eights divide by 128. The 2nd step is declare A =128. The 3rd step is A – Character representation gives you the amount of padding you can use which represents character representation. because I am allowed a total of 128 characters using the method and adding the padding I can now extend my security keys to 128 characters.

Chapter 4

Menu Screen

Date mm/dd/yyyy/ade **16384 Bits Menu Screen**

Barrys Scientific Based Products BIOS Software

Bios Chip ver 1.3

1). CPU 128 Bits

2). CPU 256 Bits

3). CPU 384 Bits

4). Password Security

5). Raided Disk

6). Hard Disk Encryption

7). BIOS Menu Encryption

8). Memory Encryption

9). USB Device Encryption

Bios Menu Screen Updates ver 1.3

The following updates have been applied for this Bios Menu Screen

1). Screen is encrypted using 16384 Bits.

2). Devices Memory and USB have now been added in this version.

3). The Date Field has been added with a extension ade meaning “after domination encryption”. This will protect against server misconfigurations do to date fields.

Higher Grade Versions will be updated and other items added to the Menu screen on the Bios.

Chapter 5

Hard Disk and Memory Encryption

After reviewing Chart 3-a, I can now create Hard Disk and Menu Screen Encryption because I have a BIOS chip that has a builtin Network Topology Hardware and System level software based on the following parameters:

1). Bios Pins 128 Pins
2). assigned variable 16384 Bits

The Equation is 16384 bits / 128 = 128 cycles based on the hardware using thick wires it would take 128 cycles to encrypt the hard disk and now Memory Chips. This would create bottle necks. The solution is to create two area buffers to load the cycles into the Data Pipe meaning each buffer could load 64 cycles since there are two and would equal 128 cycles. This would alleviate bottle necks by using the I/O scheduling mechanisms for each buffer.

Chapter 6

Final Thoughts

This is the final update for this Bios chip and was designed for low end to Middle range servers using 128, 256, and 384 Bit CPU's.

The Bios chip design offers better security than most servers in this class out in the market because of the security keys that must match the CPU and it's number of bits maximum 16384 bits. This design has a built in recovery system whereas if one security key fails you still have two other security keys. The security key encryption with the padding is now using a newly designed mathematical process and or method working with 128 bits. In previous works, I used the newly designed process and it is now valid because it has been shown to work on two different occasions. I have updated the Menu Screen using this BIOS chip at 16384 bits encrypted.

The BIOS chip uses 128 pins with the backside of the chip using a thicker internal fiber optic ring topology that utilizes encryption to protect the BIOS software. I have created two buffer areas that would allow for hard disk, memory, and USB encryption using 16384 bits. The design would be geared more to Unix or Linux based systems not built on application interfaces like Microsoft for example. The chip offers a selection of 3 different CPU's as a selection based on previous CPU designs I have written.

I would like to thank each and everyone of you for viewing this work !

If you wish to see further work please go to the following website below:

www.barrysscientificbasedproducts.com

Email bcrouse@protonmail.com

03/17/2023

Barry L. Crouse

Barrys scientific Based Products is a service mark of Barry L. Crouse registered in Washington, Idaho, and Canada.